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Novel presentation of majority gates by placing silicone and CNTFET transistors

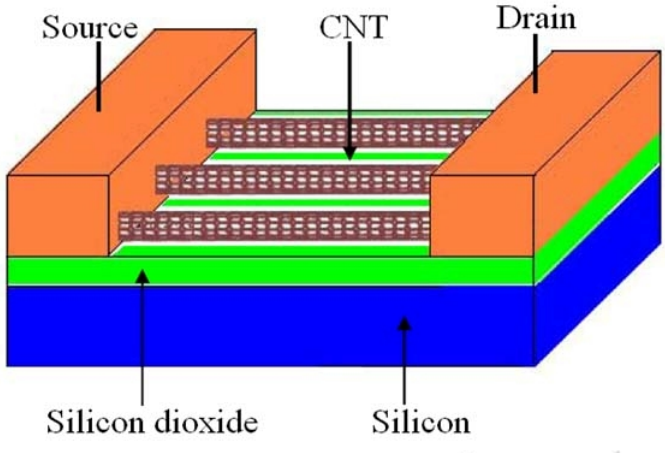
Amir Shadmanpour[1*],Peiman Keshavarzian[2]
[1, 2] Department of Computer Engineering, Kerman Science and Research branch, Islamic Azad University, Kerman, Iran.
E-mail :amir.shadmanpoor@iauk.ac.ir

ABSTRACT
In this paper, we proposed two new majority circuit designs by using mosfets and CNTFETs. We present the first circuit design with 12 transistors. In the first circuit design N-type and also P-type transistors are used to achieve a novel majority circuit design. By replacing ancient silicon technology to the novel technology (carbon nanotube field transistors) CNTFET.We have achieved best circuit parameters than the mosfet technology. The simulation results show that we have achieved an improvement in area, delay, power dissipation and PDP, respectively.
***Key words**: CNTFET Majority, New Majority, Carbon nanotube, Majority-12T, quick Majority*

INTRODUCTION

In MOSFET transistors, according to the channel in which they are formed, Nmos or Pmos called [1]. Beginning work on transistors, pmos versatile than the nmos, but then nmos over took the pmos, because the nmos was easier to build than pmos and also would occupy less space. As regards, the mosfet transistors have only one carrier (electron or hole) in the links [2]. Since, this is called unipolar transistors. FETs are made by drain, source and gate terminals which gate terminal controls the current through the drain-to-source [3]. You can see in figure 1 view of the n-type and p-type transistors. In n-type transistors, when applied voltage to gate is 1 logical value, flow passes from the drain to source and in p-type transistors, when applied voltage to the gate is 0 value, drain connected to the source and current is passed [4] [5].

Fig. 1: Circuit symbol of a-type and p-type



Nanotubes are sheets of carbon atoms which they are moving within part of the like rollers and they seem like a wire mesh. Carbon nanotubes make from carbon source such as graphite or hydrocarbon gases by methods such as electrical discharge, TCVD and laser ablation [6]. This material due to have properties such as large specific surface, high strength and unique electronic and electrical properties has been used in the manufacturing of electronic components. They are 10 times stronger than steel, whereas weight is

one-sixth the weight of steel. The only problem is that, the largest nanotubes ever made is only a few millimeters. But this ideal for small devices specially carbon nanotubes. Nanotubes are two parts : multi-wall carbon nanotube and single-wall nanotube. Multi-walls are made of graphite fibers, whereas, a single-wall carbon nanotubes are formed by
drawing fibers fullerene. Figure 2 (a) shows the schematic diagram of a carbon nanotube transistor and you can see in figure 2 (b), the two types of carbonnanotubes [7].

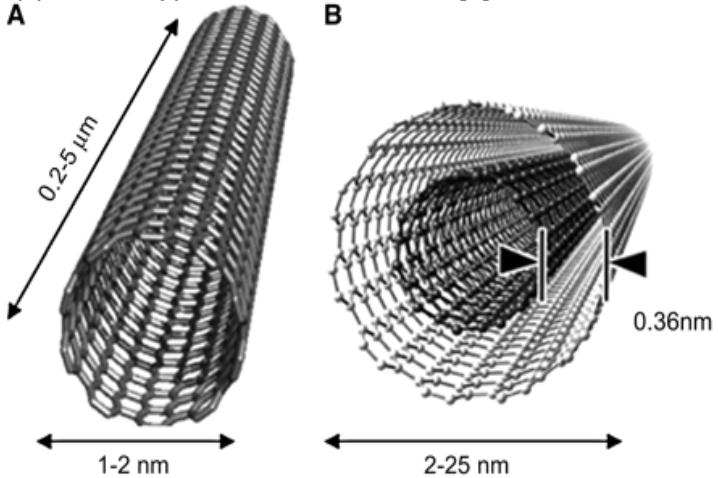


Fig. 2: (a). Schematic diagram of a carbon nanotube transistor (b). Carbon nanotube in CNTFET circuits

Single-wall CNT consists of a cylinder shaped wall which is made of graphite and has a diameter of 1 to 2nm. Multi-wall CNT consists of a thinner wall. The walls of the cylinders are 34nm of each other. The diameter of the outer wall of the multi-wall CNT is 2 to 25nm [8].

MATERIALS AND METHODS

A CNT can be single-walled carbon nanotube (SWCNT) or multi-wall carbon nanotube (MWCNT). Electrostatic contacts between plates may be cause the electrical properties of graphite are independent. Due to the vector chiral a SWCNT can be viewed as a graphite sheet. Two important features of nanotubes which the setting up of carbon atoms in the microelectronics obtained are: First, ballistic electrons can pass through the tube. Second, carbon nanotubes can change the angle of twist in the graphite layer conductive and semi-conductive.

Characterization of carbon nanotubes by chiral vector (channel) and the equation (1) is escalated:

$C_h = n_1\bar{a}_1 + \bar{a}_2 n_2$ (1)

Where $\bar{a}_1$ and $\bar{a}_2$ are a unit lattice of carbon atoms and positive. Integers (n_1, n_2) to determine the chirality tubes used. The purpose of $C_h$is environed mental CNT. (Deng, 2007)

$C_h = a\sqrt{n_1^2 + n_2^2 + n_1 n_2}$ (2)

The lattice constant (a) is calculated by using the following formula here : d=1. 44 and A is the distance between the carbon atoms in a hexagonal network.

3d = 2.49A (3)

And also the threshold voltage of carbon nanotube channel is calculated from the following equation :(Raycharchury and Ray, 2004; Bokkim et al, 2009)

$V_{th} = \frac{0.43}{d\ (nm)}V$ (4)

The diameter of carbon nanotubes obtained by the following formula :

$D_{CNT}=Ch / \pi$ (5)

The Basic Majority Circuit Design

The majority circuit design by using mosfet transistors and CMOS technology which including 3 NAND gate which has 2 inputs and 1 NOR gate which has 3 inputs and also 4 levels. Figure 3 shows the basic majority circuit design.

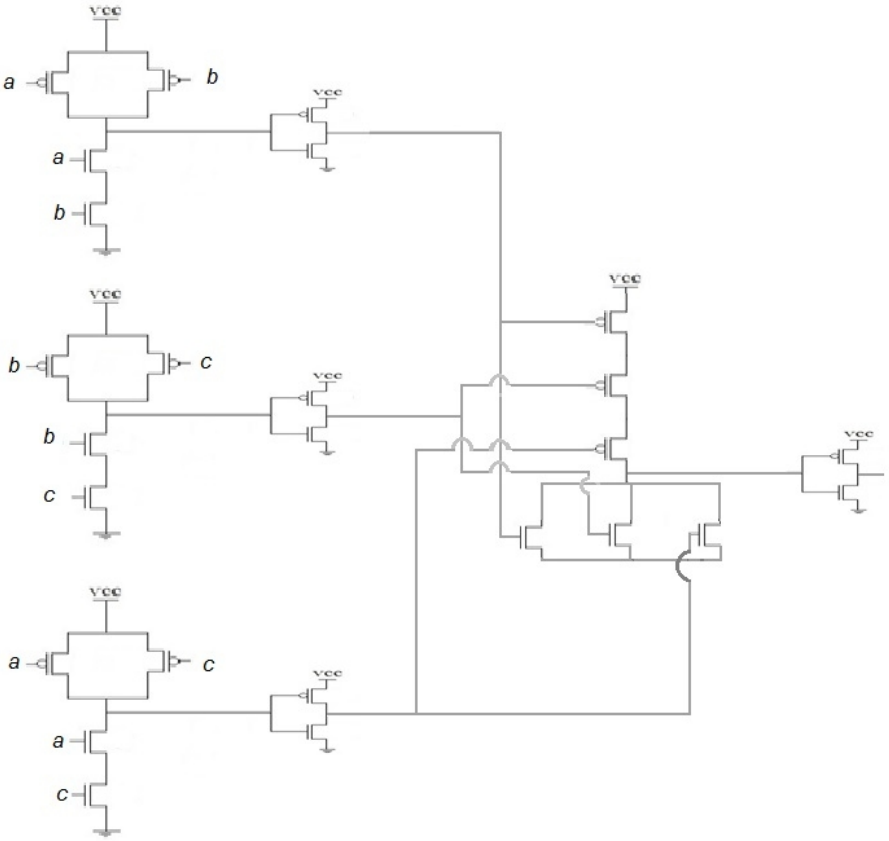


Fig. 3:Schematic diagram of basically circuit design of silicon majority gate

The Proposed our silicon majority design

The basic majority design is presented by using the ab + bc + ac function when a, b and c are the inputs. It includes 3 AND gates and also 1 OR gate. Some details about the gates are described below:

AND gates:

Each AND gate includes '2' inputs. Moreover any of them is made by 6 transistors. Totally, the gates perform by using 18 transistors.

OR gates:

We have only 1 OR gate which has 3 inputs and 1 output. The presented OR gate consists of 8 transistors. According to the details above, we need 26 transistors to design this circuit.

A majority with 3 inputs is proposed, which are a, b and c. (Table I).

The true table can be divided in two parts. If we have a=0 the output achieved by using the (band c) functions. And if we have a=0 the output achieved by using the (b and c) functions.

Table 1

a	b	c	Out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

In this paper, because of its better performance we used the NN-mos transistors as the pull down and P-mos as the pull up to ensure that our circuit design. A major function operates within inputs (which n should be added) and prepare us an output in this paper we proposed 3-input majority function. All the majority inputs and outputs are binary, so that if we have more than two "even" the output will be equal to "even", and if we have more than two "odd" the output will be equal to "odd". In our circuit design, we

divided our work in two different parts. The first part operate as a NAND gate and it will be activated when a=0, the second part operate as a NOR gate that will be activated when we have one at a. When p5 is ON, the output of the NAND gate (out5) will be connected to the input of the NOT gate (p6, n6), when n5 is OFF, out5 will be disconnected. In the first level of our circuit we have a NAND and a NOR cmos gate which will be connected to the output by using the "a" input. Figure 4 shows our proposed the first circuit design.

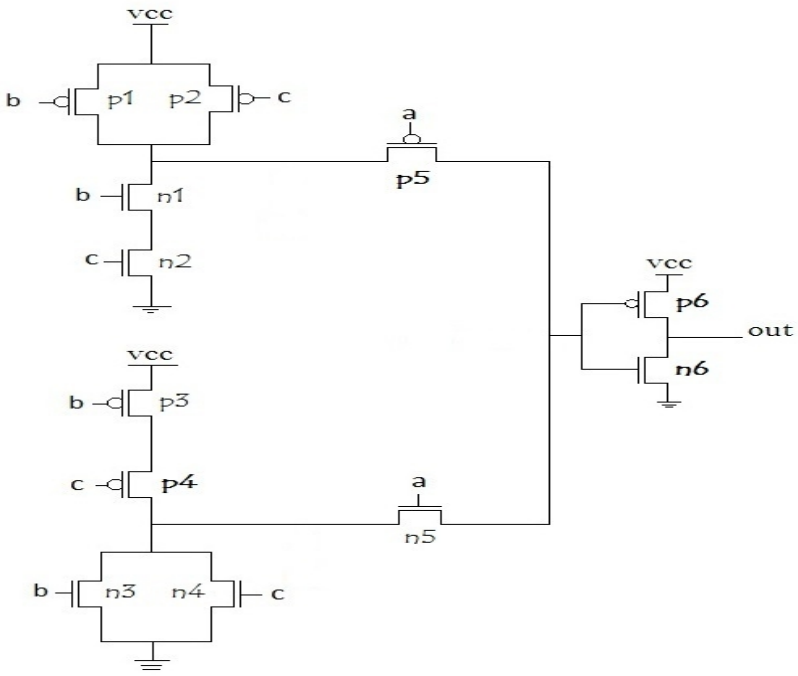


Fig. 4: Schematic diagram of proposed our silicon majority design

Our Proposed carbon nanotube field effect transistors (CNTFET) majority design

By replacing mosfet to CNTFET a significant improvement in delay, power consumption and PDP will be achieved. Figure 5 shows the second proposed circuit design

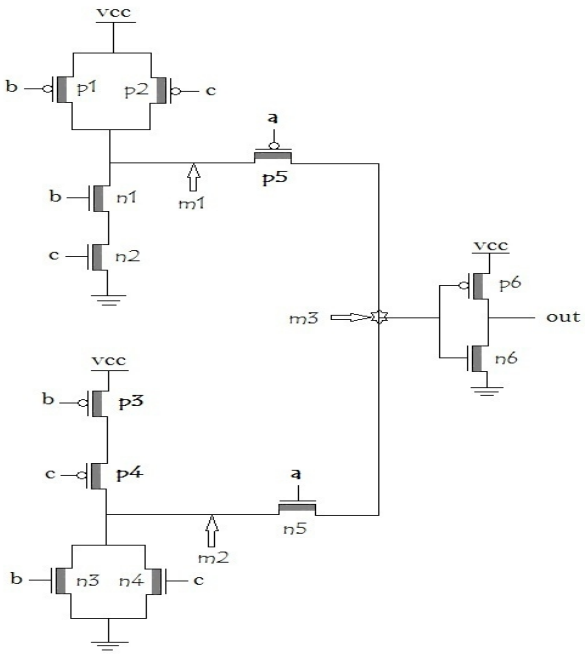


Fig. 5: Schematic diagram of proposed ourCNTFET majority design

RESULTS AND DISCUSSION

Figure 6 shows simulation results of basic majority circuit design. We have simulated this majority gate with voltage of 0.9v and room temperature of 15° C.

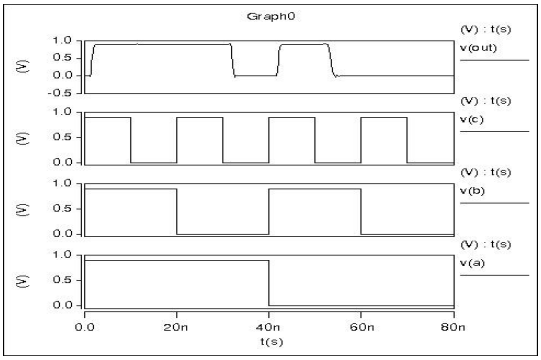
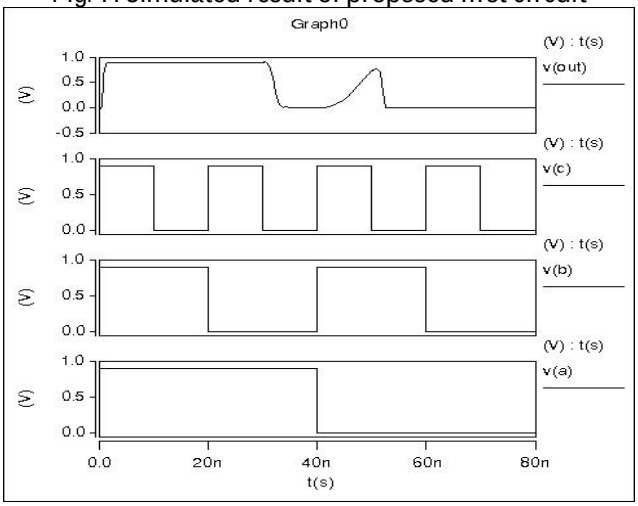


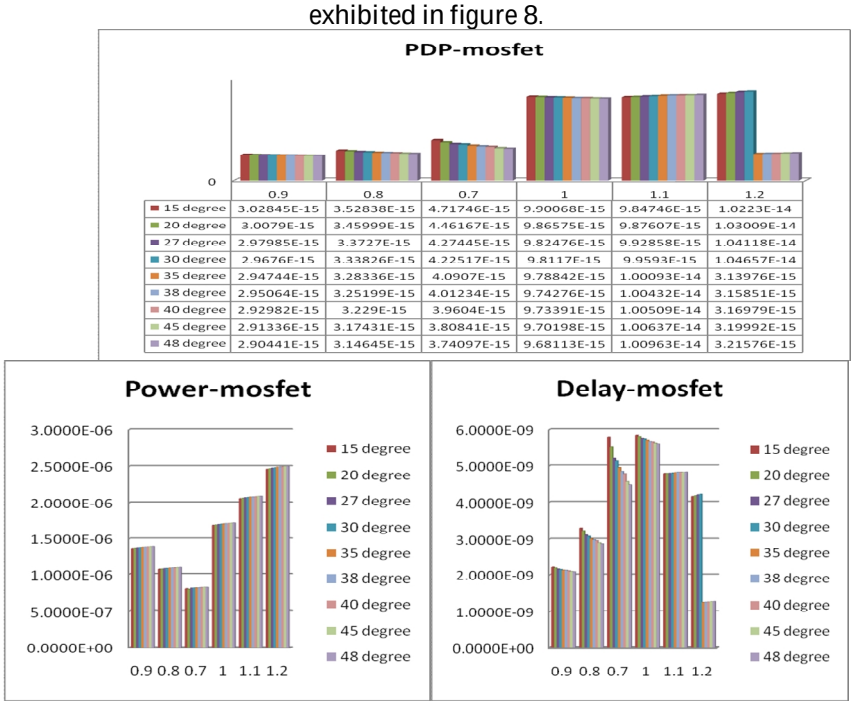
Fig. 6: Simulated results of the basic majority circuit design

Also figure 7 exhibited simulation result of our majority cmos circuit.

Fig. 7: Simulated result of proposed first circuit



The simulation results of the delay, power and PDP of the first proposed circuit in different temperature exhibited in figure 8.



	0.9	0.8	0.7	1	1.1	1.2
15 degree	3.02845E-15	3.52838E-15	4.71746E-15	9.90068E-15	9.84746E-15	1.0223E-14
20 degree	3.0079E-15	3.45999E-15	4.46167E-15	9.86575E-15	9.87607E-15	1.03009E-14
27 degree	2.97985E-15	3.3727E-15	4.27445E-15	9.82476E-15	9.92858E-15	1.04118E-14
30 degree	2.9676E-15	3.33826E-15	4.22517E-15	9.8117E-15	9.9593E-15	1.04657E-14
35 degree	2.94744E-15	3.28336E-15	4.0907E-15	9.78842E-15	1.00093E-14	3.13976E-15
38 degree	2.95064E-15	3.25199E-15	4.01234E-15	9.74276E-15	1.00432E-14	3.15851E-15
40 degree	2.92982E-15	3.229E-15	3.9604E-15	9.73391E-15	1.00509E-14	3.16979E-15
45 degree	2.91336E-15	3.17431E-15	3.80841E-15	9.70198E-15	1.00637E-14	3.19992E-15
48 degree	2.90441E-15	3.14645E-15	3.74097E-15	9.68113E-15	1.00963E-14	3.21576E-15

Fig. 8: Simulated results of delay, power and PDP of proposed first circuit

Fig. 8: Simulated results of delay, power and PDP of proposed first circuit

figure 9 exhibited simulation result of the carbon nanotube majority circuit. This circuit simulated at temperature 27° C and 0.9v.

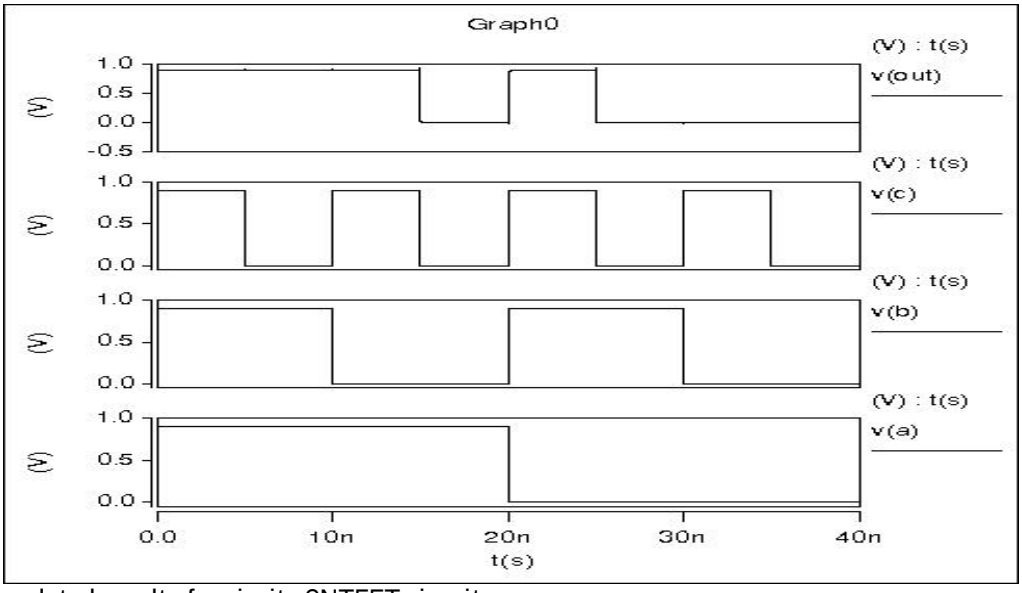
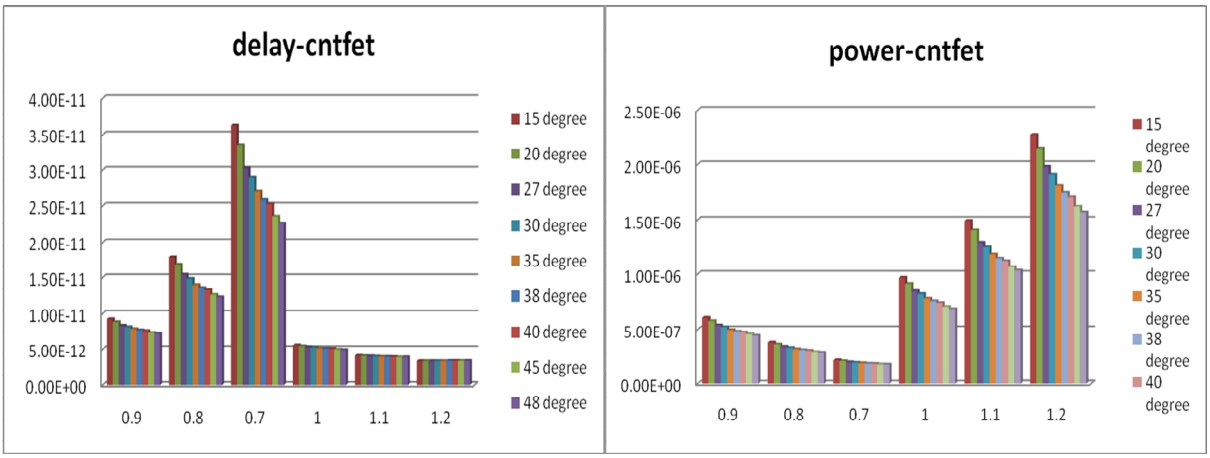


Fig. 9: Simulated result of majority CNTFET circuit

The simulation results of the delay, power and PDP of the proposed second circuit design in different temperature exhibited in figures 10.



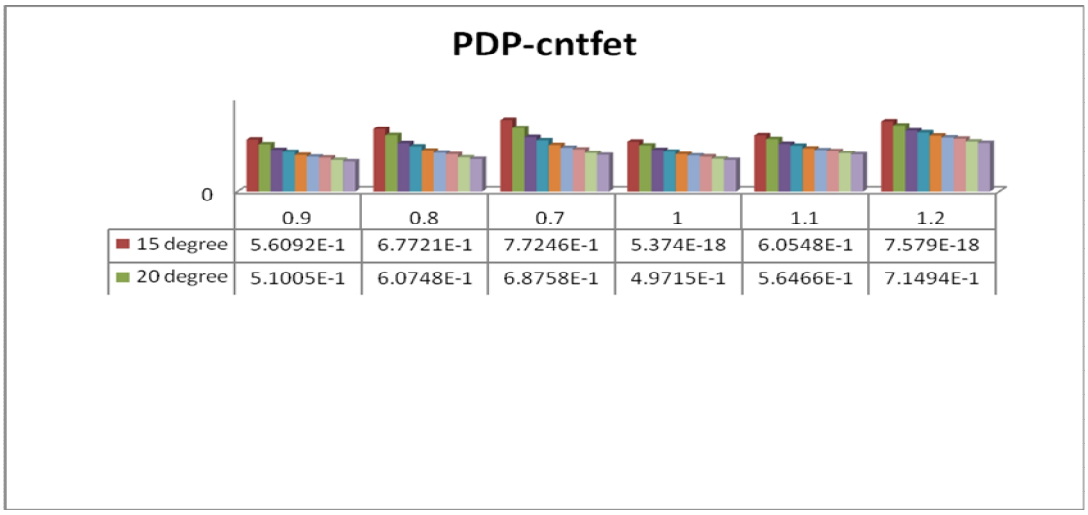


Fig. 10: simulated results of delay, power and PDP proposed second circuit in different temperature

Finally, we represented the simulation resultcomparison as the gallows. Figure 11 shows the difference between delay, power dissipation, PDP and area by the simulation our proposed circuit design in 0.9 v and temperature of 15° c.

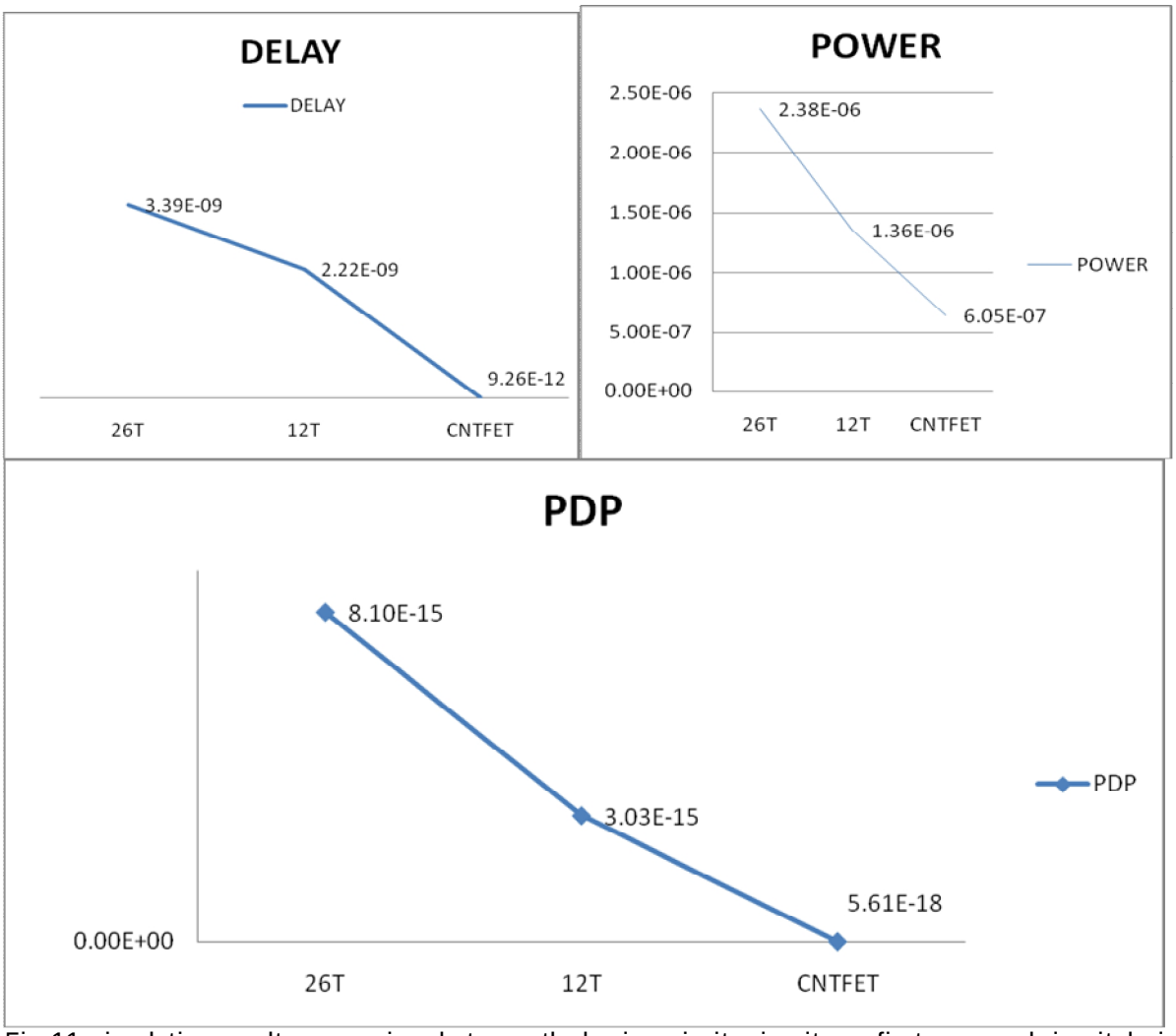


Fig. 11: simulation results comparison between the basic majority circuit, our first proposed circuit design and the second proposed circuit design

CONCLUSION

In this paper, we presented novel majority circuit designs. In the first circuit design, majority gate using mosfet transistors which improved delay up to 37%, power dissipation up to 42%, PDP up to 64% and area 53% than the basic majority circuit design. In the second circuit design, we replaced the mosfet transistors in the CNTFET transistors which improved delay up to 99%, power dissipation up to 60%, PDP up to 99% than the first proposed circuit design.

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