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ORIGINAL ARTICLE

A New High Accuracy and Resolution Flash TDC Based on Interpolation and Time Stretching

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ABSTRACT
In this paper a new flash time to digital converter that employs interpolation and time stretching techniques for digitizing the time interval input signals and increasing resolution is presented. In the proposed converter, interpolation is performed based on the dual slop conversion. The proposed converter features high accuracy, very small average error and high resolution. Also this converter has advantages of high speed conversion, low sensitive to the temperature; power supply and process variations (PVT), eliminating the comparator offset voltage error and eliminating the comparator parasitic capacitors error compared with the time to digital converters that used preceding conversion techniques. Also, due to the use of flash structure, the proposed converter has advantage high conversion rate. The proposed converter circuit is simple and its resolution is achieved from the difference between the voltages or the charge stored in the capacitors in flash structure. In order to evaluate the proposed idea, a flash time to digital converter is designed in TSMC 0.18µm CMOS technology and was simulated by Hspice. Comparison of the theoretical and simulation results confirms the proposed TDC operation, so it can be used for high speed and resolution applications.
Keywords: *Time to Digital converter (TDC), Interpolation, Time Stretching, Dual slop conversion, Indirect time to digital conversion.*

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INTRODUCTION

In recent years, time to digital converters have wide applications in industry such as on-chip time signal measurement, biochemical sensor readout and frequency synthesis circuits [1], All Digital Phase Locked Loops (ADPLL) [2,3], Laser range finders [4], digital storage oscilloscopes and capacitive sensor readouts [5]. In the time to digital converters, the time interval between the rising edges of the input signals, Start and Stop, can be measured analogically, digitally or using interpolation techniques [6]. Analog method is based on charging or discharging the capacitors in the interval between Start and Stop signals by a constant current source. Accuracy in this method is excellent but is suffers from poor stability and linearization. Therefore, its measurement range is usually short [6]. The digital method is based on synchronous counting clock cycles of a reference oscillator. It is linear over a wide measurement range, but its precision is limited by the uncertainty attached to ±1 clock cycle. A higher resolution can be obtained by raising the clock frequency, but more power is consumed [6].

In general, the time to digital converters can be classified into two parts: the direct and indirect conversion schematics [7]. In the time to digital converters with direct conversion, the delay lines are used to measure short time intervals between the rising edges of the input signals, Start and Stop [8,9]. The main disadvantages of these converters are complex circuit structures and hence the high power consumption, high sensitivity to variations in the process parameters, supply voltage and temperature (PVT) [6]. When a mismatch occurs between these converters' elements, nonlinear factors appear in their operation and equations. In general, the dynamic range of these converters is limited by the number of delay stages which leads to slow conversion rate [10]. Time to digital converters with indirect conversion can be divided into two parts. First, the converters that are included a time to analog conversion stage and an analog to digital conversion stage. The ramp time to digital converters [11] and dual slop pulse

stretching time to digital converters [12,13] are two types of these converters. Because there are several conversion steps, this kind of converters are low-speed. Second, there are converters that take advantage of interpolation techniques for conversion [6,14,15]. The interpolation techniques are indirect techniques for time to digital conversion. The interpolation circuits are usually united with the counter based time to digital converters to increase the input range to infinity [6]. In compared with similar structures, this approach reduces chip area and therefore reduces power consumption. The proposed converter in this paper is a counter based time to digital converter. In [6,14] is presented two interpolation methods for time to digital conversion. Due to the using of capacitors in parallel with the comparator inputs, the offset voltage and parasitic capacitances errors in the comparators arise. Also, in these converters, the resolution is dependent to capacitors ratio and current sources ratio. Thus, the element's mismatches affect the TDC resolution and accuracy. In [14], the chip area increases because it uses a decoder and digital counters in the converter structure.

In this paper a new flash time to digital converter is presented. It employs the interpolation and time stretching techniques for digitizing the time interval between input signals and increasing resolution. In the proposed converter, interpolation is performed based on the dual slop conversion. The time interval between the input signals is coarsely measured by the main counter with an accurate reference clock. The fractional portions at the beginning and ending of the input are interpolated by two separate time digitizers to improve the time resolution of the TDC.

This paper organized to the following: The second section presents the background of the dual slop time stretching time to digital converter. In the third section, the scheme circuit and the operation modes of the proposed converter is described theoretically. The fourth section shows the results of simulation by Hspice in the TSMC 0.18µm CMOS Technology. Fifth, the results of the two previous sections are compared with each other.

Basic Principal

In this section, the principal operation of the dual slop time stretcher time to digital converter is introduced and the different modes of operation of the converter are investigated.

Dual slop time stretcher based time to digital converter

The block diagram of the TDC based on the dual slope time stretching technique is shown in Figure 1. It's a counter based time to digital converter and uses interpolation technique to increase the resolution [14]. It consists of a time to pulse generator (or a time splitter), a coarse counter, two parallel dual slope time stretchers, two fine counters (or two parallel dual slope time stretchers), an encoder and several logic elements. The time to pulse generator block diagram and its timing diagram is shown in Figure 2(a) and 2(b) respectively. In the time to pulse generator, the time interval between the rising edges of the input signals, T_{in}, are digitized into three separate parts, T_1, T_2 and T_{12}. The main part, T_{12}, is related to coarse measurements and can be digitized by a main counter with an accurate synchronous reference clock, CLK. Also, the fractional periods, T_1 and T_2, are digitized by the analog interpolators with the finer resolution than T_{Clk} [14]. If the analog interpolators numbers of bit are equal to n, thus, the time interval between two input signals, T_{in}, is obtained by:

$$T_{in} = D_{12} \times T_{Clk} + (D_1 - D_2) \times \frac{T_{Clk}}{2^n} \quad (1)$$

where $T_{Clk}/2^n$ is time to digital converter's LSB. Also, D_{12} is digital output of the main counter and D_1 and D_2 are the digital outputs of the analog interpolators 1 and 2 respectively.

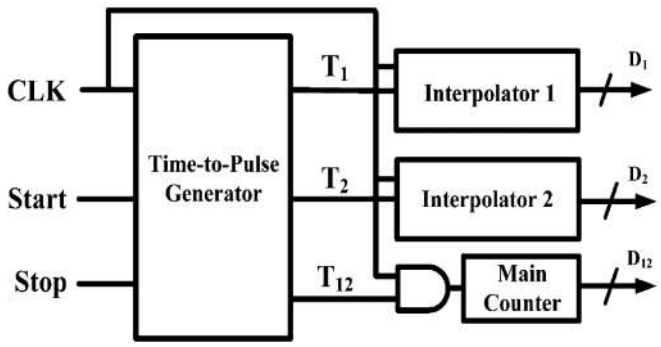


Figure 1. The block diagram of the TDC based on the dual slope time stretching technique in [14]

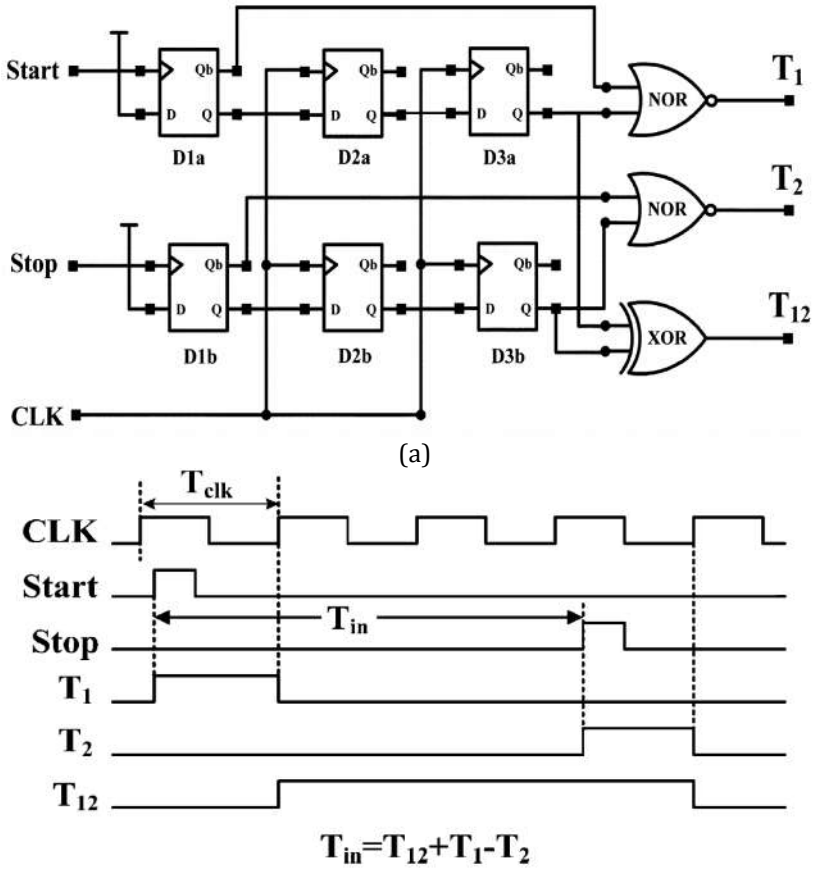


Figure 2. Time splitter (a) circuit structure and (b) timing diagrams for a dual slope time stretcher based TDC in [14].

Two parallel dual slope time stretchers, analog interpolators, and its timing diagram that is described in [14], are shown in Figure 3(a) and 3(b) respectively. Briefly, the converter performance is: Initially, both capacitors, C_1 and C_2, charge to up. In rising edge of T_1, smaller capacitors, C_1, is charged by the grater constant current source, I_1. This mode ends at the falling edge of T_1. The falling edge of T_1, the grater capacitor $C_2 = M.C_1$, began to discharge by the smaller constant current source, $I_2=I_1/N$. Discharging the capacitor C_2 is done by the reference clock, CLK1, which has the duty ratio less than 1, 1/P. Therefore, The corresponding stretch factor becomes $(M.N.P)$ and the LSB width of the TDC is $T_{Clk}/(M.N.P)$.

So the time interval between the input signals is measured as:

$$T_{in} = D_{12} \cdot T_{Clk} + (D_1 - D_2) \cdot \frac{T_{Clk}}{(M \cdot N \cdot P)} \quad (2)$$

Thus, this converter can improve the resolution and reduce the power consumption. But this converter has several problems. First, the converters that are introduced in [6] and [14] have
the offset voltage error, because they employ the capacitors that are in parallel with the comparators inputs. The offset voltage error makes the pulse width of the comparator output incorrect.

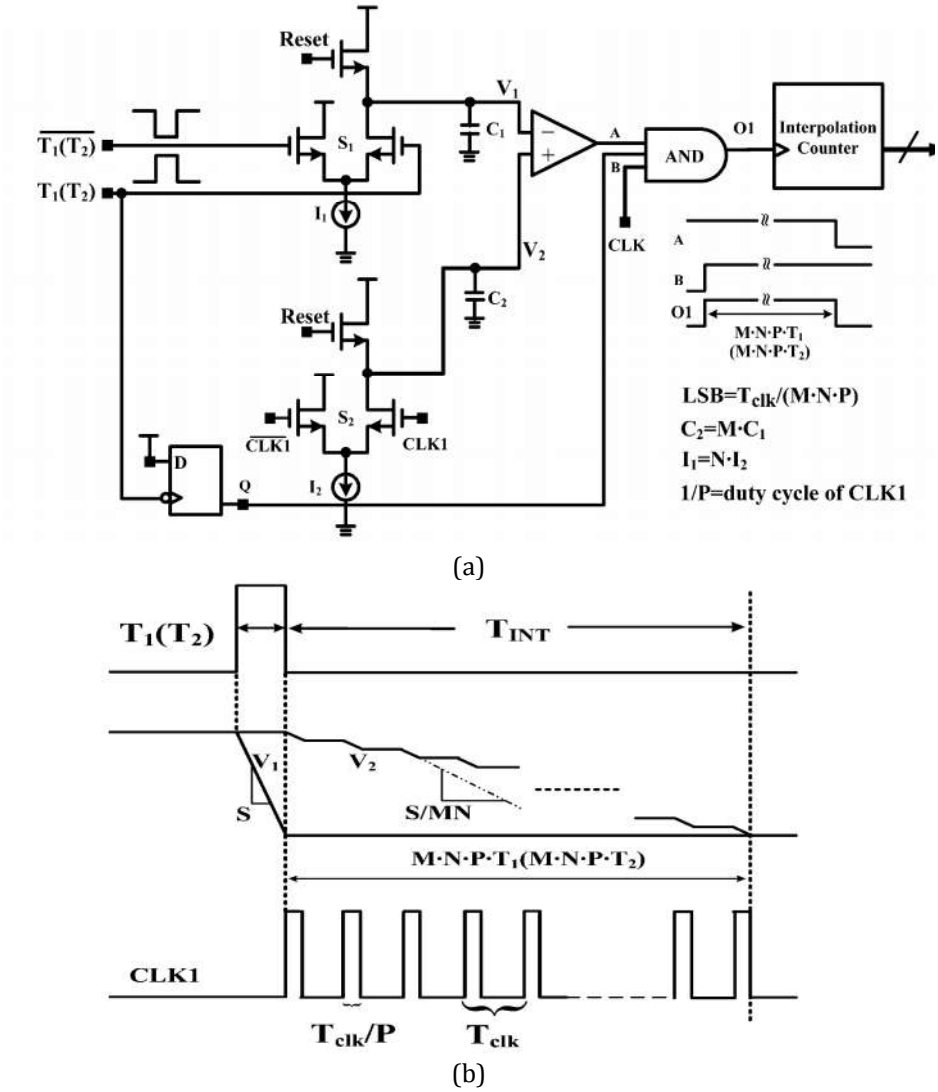


Figure 3. (a) Block diagram and (b) timing diagram of dual slope time stretchers analog interpolator in [14]

As a result, interpolation counters produce an incorrect count. The resolution is higher; the comparator offset voltage error is greater. Thus, the accuracy of the converter is reduced. Second, the converters that are introduced in [6] and [14] have the comparator parasitic capacitors, because they employ the capacitors that are in parallel with the comparators inputs. The parasitic capacitors in parallel with C_1 and C_2 make the capacitors ratio, M, inaccurate. Third, more than 80% of chip area has been allocated to two parallel dual slope time stretchers structures in [6]. Also, the large capacitor increases the occupied chip area. Fourth, the introduced converters in [14] and particularly [6] have low conversion speed compared with the converters that apply direct conversion methods and the converter with high speed conversion method such as flash structure, because they use the multi stage structures and multiple logic gates for time to digital conversion.

The Proposed flash Time to digital converter

This section investigates the performance of the proposed converter in different modes of operation. The proposed analog interpolator circuit and the theoretical waveforms are shown in the Figure 4 and Figure 5 respectively. In the Figure 5, V_{CX} is the voltage of the each capacitors, C_1, C_2, …, C_n and O_X is the output of the each comparators, O_1, O_2, …, O_n. In the proposed converter, interpolation is performed based on the dual slop conversion.

Mode 1:

Initially, all capacitors in the analog interpolator circuit are charged to up. In this mode, M_{13} to M_{20} transistors switches are on, thus, all capacitors are charged to up.

Mode 2:

Mode 2 starts in the rising edge of T_1. In this mode, the small capacitor, C_k, is discharged by the greater constant current source, I_{ref1}, linearly. $I_{ref1}=G.I_{ref2}$. The voltages of C_1 to C_n remain same in during of this mode. Thus, the comparators outputs are zero in during of this mode. This mode ends in the falling edge of T_1. In this mode, the equation of the discharging C_k is obtained by:

$$I_{ref} \times T_1 = C_k \times (V_{up} - V_P) \quad (3)$$

where V_p is the voltage of C_k at the end of this mode.

Mode 3:

Mode 3 starts in the falling edge of T_1. The interpolation counter is enabled. In this mode, the control switches, S_1 to S_n, are turned on by the reference clock, CLKD, periodically. In each period of CLKD, C_1 to C_n are discharged whit different time constants. The duty ratio of CLKD is set to be greater than 0.5 to further slow down the discharging speed. The capacitors discharging are performed by transistors with different sizes, M_1 to M_n. In the proposed analog interpolator, there are different ways for discharging each of the capacitors, C_1 to C_n. The proposed converter has the same comparators in the output stage. The number of comparators is greater, the resolution is improved. In each period of CLKD, C_1 is discharged with $\tau_1 = R_1 \times C_1$ time constant. Similarly, C_2, C_3, ... and C_n are discharged with $\tau_2 = R_2 \times C_2$, $\tau_3 = R_3 \times C_3$, ... and $\tau_n = R_n \times C_n$ time constants respectively. In these equations, R_1 to R_n are the transistor resistors, M_1 to M_n, respectively. These transistors operate in the linear region. Transistor resistor is inversely proportional to its size. In the proposed converter, the values of capacitors, C_1 to C_n, are the same and $K.C_k$. the discharging capacitors equations, C_1 to C_n, are obtained by:

$$V_{C_X}(t) = V_{up} \times e^{-\frac{t}{R_X C_X}} \quad and \quad X = 1,2,3,\ldots,n \quad (4)$$

To obtain the resolution in the proposed converter, the following equation is satisfied where all comparators outputs are low.

$$V_{Cn+1} - V_{Cn} = V_{Cn+2} - V_{Cn+1} \quad (5)$$

By substituting the equation (5) into (4), the relationship between the resistors of transistors, M_1 to M_n, can be obtained as

$$R_{n+1}^2 = R_{n+2} \times R_n \quad (6)$$

Thus, the relationship between the sizes of the transistors, M_1 to M_n, for an appropriate resolution are obtained as

$$\left(\frac{W}{L}\right)_{n+1}^2 = \left(\frac{W}{L}\right)_n \times \left(\frac{W}{L}\right)_{n+2} \quad (7)$$

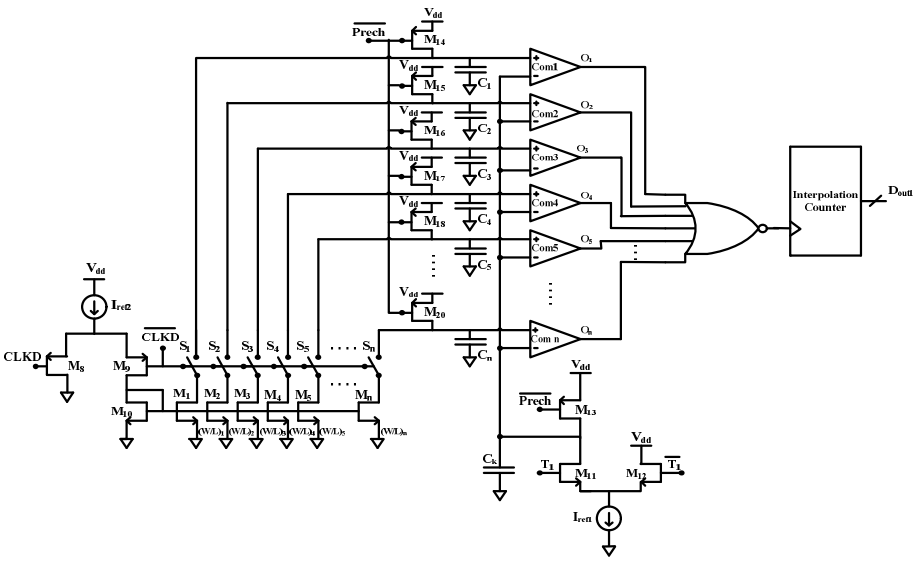


Figure 4. The proposed analog interpolator circuit

The time interval between input signals, T_{in}, is divided to two parts, T_{Coarse} and T_{Fine}. Thus

$$T_{in} = T_{Coarse} + T_{Fine} \tag{8}$$

T_{Coarse} is achieved by a main counter which has an accurate reference clock, Clk. Thus

$$T_{Coarse} = D_{12} \times T_{Clk} \tag{9}$$

Where D_{12} and T_{clk} are the digital output of the main counter and the period of reference clock, Clk, respectively. Thus:

$$\Delta V = V_{Cn+1} - V_{Cn} = \frac{T_{Clk}}{C_n \times P} \cdot (I_{n+1} - I_n) \tag{10}$$

Where V_{Cn+1} and V_{Cn} are the voltage of C_{n+1} and C_n in one period of the reference clock, CLKD, respectively. ΔV is the voltage difference of two consecutive capacitors in the proposed converter. Also, 1/P is duty ratio of the reference clock, CLKD. As well as, I_{n+1} and I_n are the currents of transistors, M_{n+1} and M_n in the linear region respectively and have difference proportion of the smaller current source, I_{ref2}. Since the transistors, M_1 to M_n, have the same coefficient, $\mu_n \cdot C_{ox}$, and the same gate-source voltage, V_{gs}, thus

$$I_{n+1} - I_n = \mu_n C_{ox}[\left(\frac{W}{L}\right)_{n+1} \cdot (BV_{n+1} - \frac{V_{n+1}^2}{2}) - \left(\frac{W}{L}\right)_n \cdot (BV_n - \frac{V_n^2}{2})] \tag{11}$$

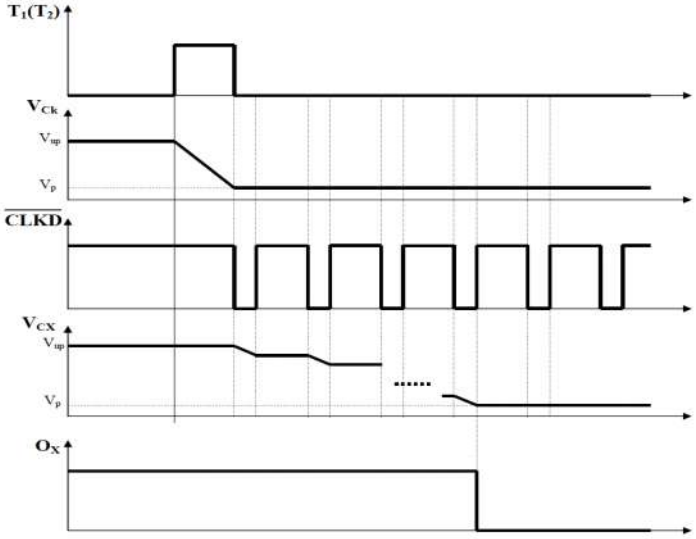


Figure 5. The theoretical waveforms of the proposed converter

where $B = (V_{gs} - V_{th})$ and V_{th} is the threshold voltage of the transistors, M_1 to M_n. Also, according to equations (10) and (11) the following equation is obtained:

$$\begin{aligned} &\mu_n C_{ox} \left(\frac{W}{L}\right)_{n+1} \cdot \frac{V_{n+1}^2}{2} + V_{n+1} \cdot (\frac{C_{n+1} \times P}{T_{Clk}} - \mu_n C_{ox} \cdot \left(\frac{W}{L}\right)_{n+1} .B) = \\ &\mu_n C_{ox} \left(\frac{W}{L}\right)_n \cdot \frac{V_n^2}{2} + V_n \cdot (\frac{C_n \times P}{T_{Clk}} - \mu_n C_{ox} \cdot \left(\frac{W}{L}\right)_n .B) \end{aligned} \tag{12}$$

In this mode, in each period of CLKD, the voltage difference of two consecutive capacitors in the positive inputs of the comparators is doubled compared with the previous period of CLKD.

This mode ends where all of comparators outputs are low. In other words, this mode ends where the voltage of capacitors in the positive inputs of comparators are greater than or equal with V_p. Therefore, the output of NOR gate becomes high and interpolation counter is stopped. In the end of this mode, the output digital, D_{out1} is produced.

Thus, T_{Fine} is

$$T_{Fine} = (D_{out1} - D_{out2}) \times \Delta T = (D_{out1} - D_{out2}) \times \frac{T_{Clk}}{(P.K.G)} \tag{13}$$

Where P and K are the duty ratio of CLKD and capacitors ratio respectively. Also, G is the current sources ratio. In (13), D_{out1} and D_{out2} are the digital outputs in the analog interpolators 1 and 2 respectively. Therefore, the stretch factor becomes (P.K.G) and the LSB width of the TDC becomes $T_{Clk}/(P.K.G)$.
As explained, the resolution in the proposed converter is obtained by calculating the difference voltage between two consecutive capacitors in two consecutive comparators. The number of comparators in output stage is greater, the resolution is improved. Thus, unlike the converters that are described in [6] and [14], the comparator offset voltage error and comparators parasitic capacitors error is not exist in the proposed converter. The proposed converter uses the flash structure for analog interpolation, so, the proposed converter has higher speed in compared with the [6] and [14]'s converters. In compared with direct structures such as delay line conversion and vernier delay line conversion, interpolation method reduces chip area and therefore reduces power consumption. Also, the indirect conversion techniques, such as interpolation technique, are advantaged low sensitive to the temperature; power supply and process variations (PVT) in compared with the direct conversion techniques.
The accuracy and resolution of the proposed converter are achieved by the difference between the voltages or the stored charges in the capacitors which in the comparators inputs into analog interpolator. Therefore, the offset voltage and parasitic capacitors errors are eliminated in the proposed converter. They are occurred in the TDC that have the capacitors in parallel with the comparators inputs and affect on the converter's accuracy and resolution. These problems exist in [6] and [14]. The proposed converter topology is simple and its linear range is high. The proposed converter is an indirect TDC. Thus, the chip area and subsequently power consumption are reduced relatively. As a result, the proposed converter is useful for applications requiring high accuracy and resolution and high speed conversion such as laser range finders, phase meters and digital storage oscilloscopes.

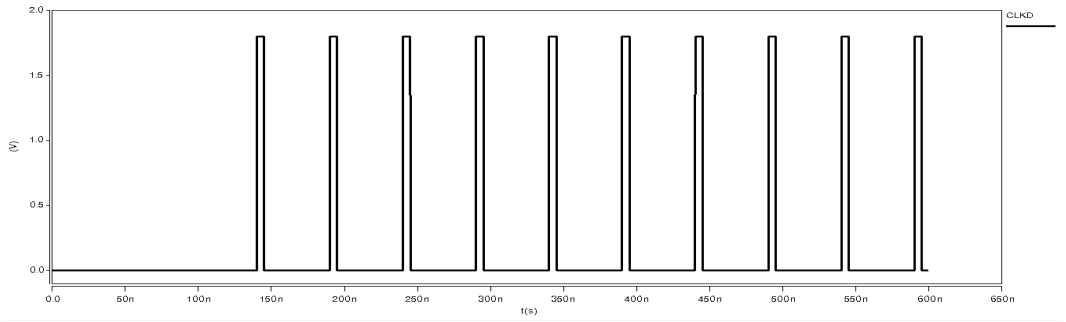
SIMULATION RESULTS

The simulation results of the proposed converter by Hspice in TSMC 0.18µm CMOS technology are investigated in this section. The simulated converter has 7 comparators in the output stage. The proposed converter is implemented by the following elements: C_k is 10nF. Also, C_1 to C_7 are 50nF. Current sources values are 200uA. The transistors, M_1 to M_7, sizes are

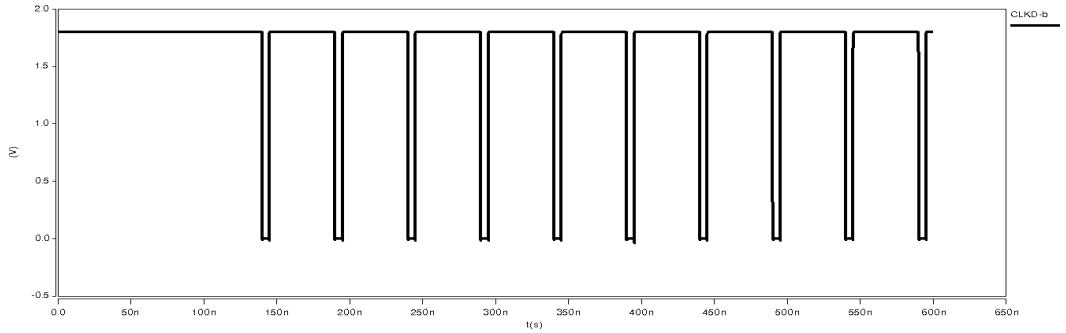
$$\left(\frac{W}{L}\right)_1=\left(\frac{17.5u}{180n}\right),\quad \left(\frac{W}{L}\right)_2=\left(\frac{14u}{180n}\right),\quad \left(\frac{W}{L}\right)_3=\left(\frac{11.5u}{180n}\right),\quad \left(\frac{W}{L}\right)_4=\left(\frac{10.2u}{180n}\right),\quad \left(\frac{W}{L}\right)_5=\left(\frac{9u}{180n}\right)$$

$$\left(\frac{W}{L}\right)_6=\left(\frac{8u}{180n}\right),\quad \left(\frac{W}{L}\right)_7=\left(\frac{7.2u}{180n}\right)$$

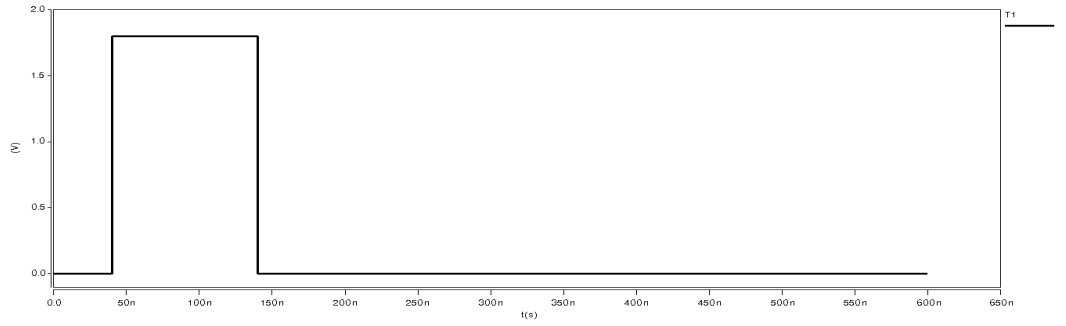
respectively. Figure 6(a), 6(b), 6(c) and 6(d) are shown the $CLKD$, $\overline{CLKD}$, T_1 *and* $\overline{T}_1$ waveforms respectively. The duty ratio of CLKD is 90%. Thus, P=10 for the converter. Figure 7 is shown the capacitors voltages waveforms. Figure 8 is shown the comparators outputs waveforms. The input time signal, T_1 (T_2) is high for 100ns. In this period, the voltage of C_k, V_{Ck}, reduces to 0.65V. The time constant of C_1 is greater than other capacitors. Therefore, the voltage of C_1, V_{C1}, reduces to 0.65V in the less number of CLKD period and the comparator output, O_1, is low earlier than the other comparators outputs. Figure 7(b) and Figure 8(a) confirm it. Similarly, the time constant of C_2 is greater than C_3 to C_7 time constants but smaller than C_1 time constant. Therefore, the voltage of C_2, V_{C2}, reduces to 0.65V in the less number of CLKD period than the voltage of C_3, V_{C3}, to the voltage of C_7, V_{C7} but in more number of CLKD period than V_{C1}. Thus, the comparator output, O_2, is low earlier than the comparators outputs, O_3 to O_7 but posterior than O_1. Figure 7(c) and Figure 8(b) confirm it. This functionality is extended to other capacitors and comparators. In the simulated converter, in 540ns all comparators outputs are low. The CLKD period is 50ns. Therefore, after ten periods of CLKD, all comparators outputs are



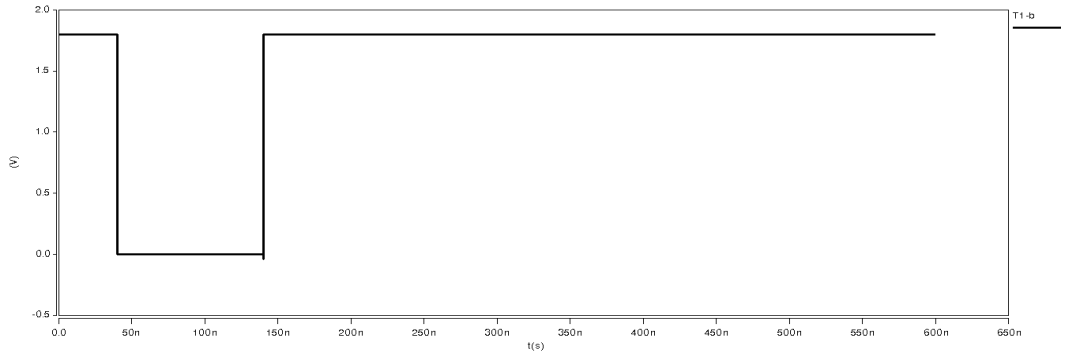
(a)



(b)

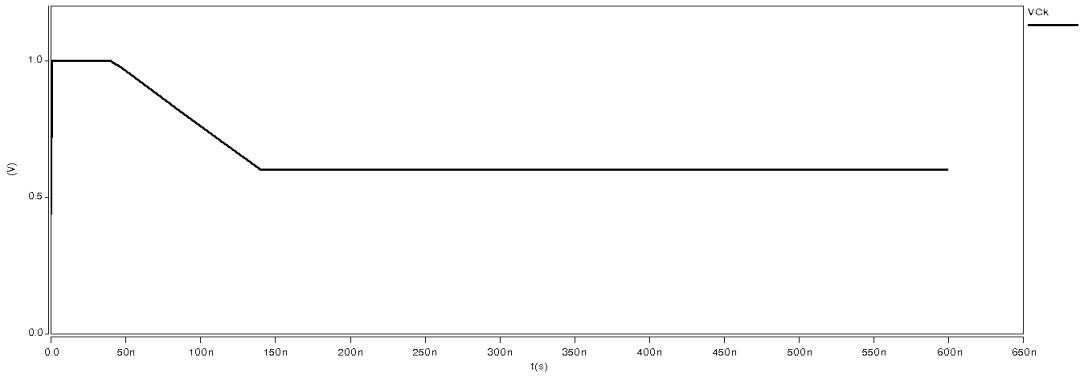


(c)

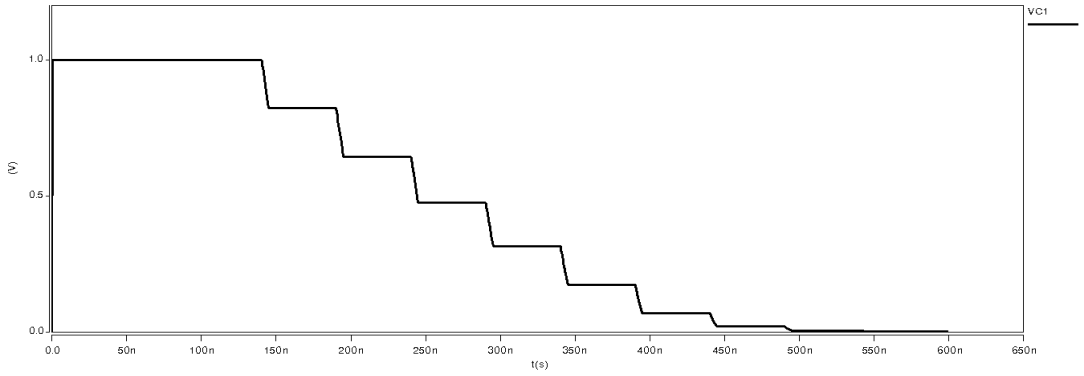


(d)

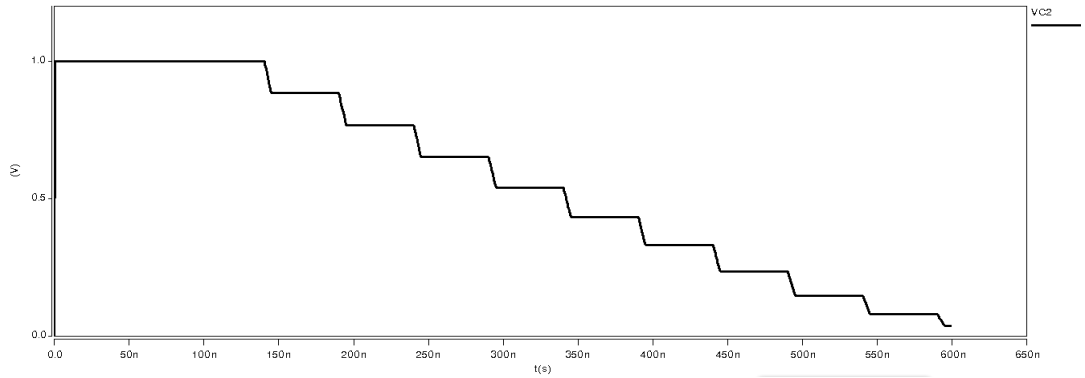
Figure 6. The time signal waveforms (a) $CLKD$, (b) $\overline{CLKD}$, (c) T_1 , (d) $\overline{T_1}$


Vck
1.0
0.5
0.0
(V)
0.0
50n
100n
150n
200n
250n
300n
350n
400n
450n
500n
550n
600n
650n
t(s)

(a)


VC1
1.0
0.5
0.0
(V)
0.0
50n
100n
150n
200n
250n
300n
350n
400n
450n
500n
550n
600n
650n
t(s)

(b)


VC2
1.0
0.5
0.0
(V)
0.0
50n
100n
150n
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250n
300n
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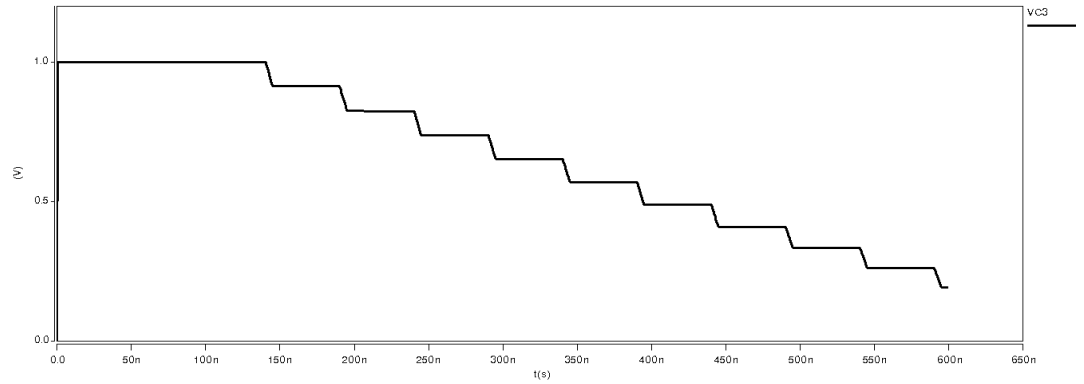
450n
500n
550n
600n
650n
t(s)

(c)


VC3
1.0
0.5
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(V)
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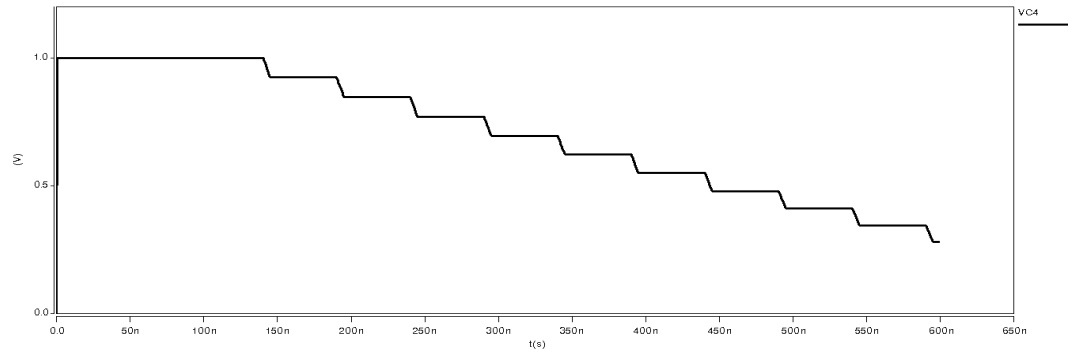
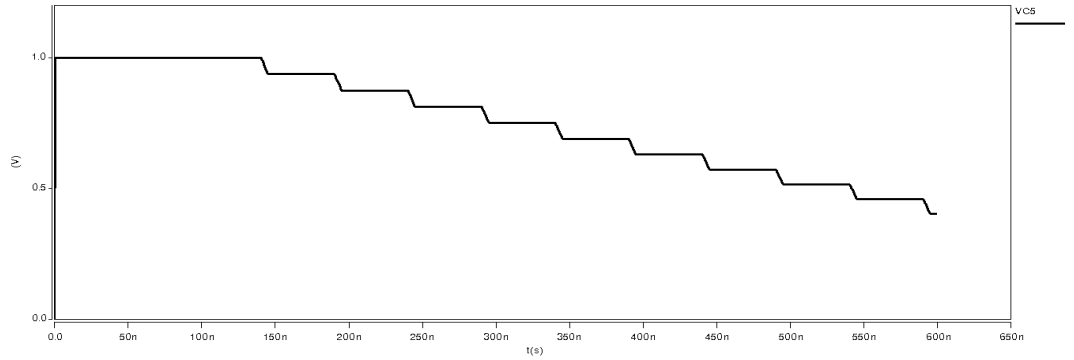
600n
650n
t(s)

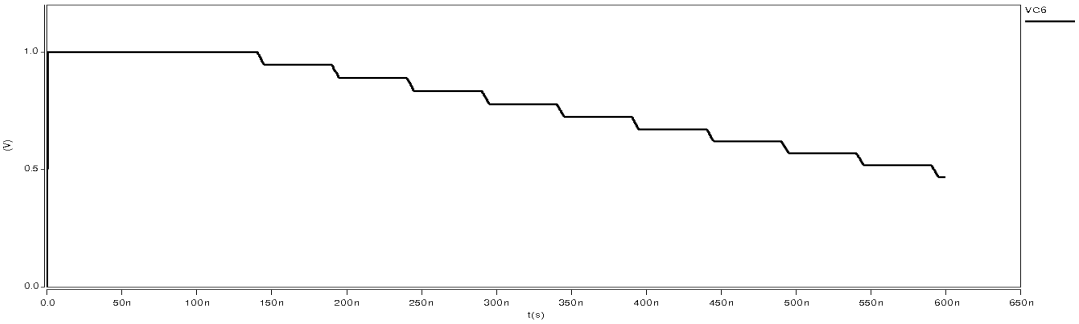
(d)



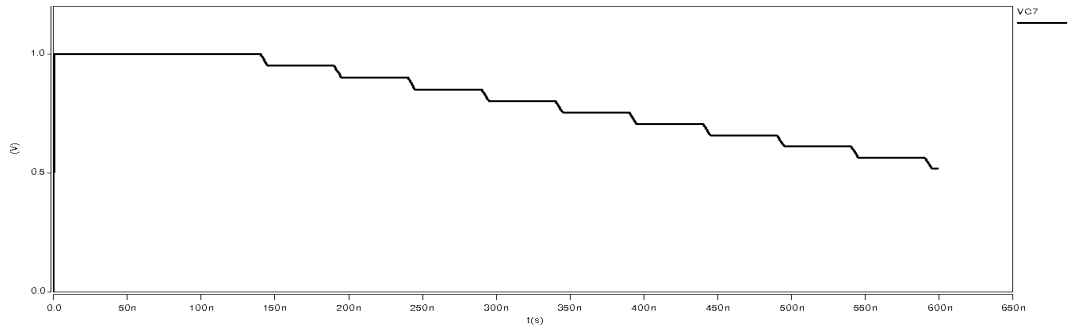
(e)



(f)

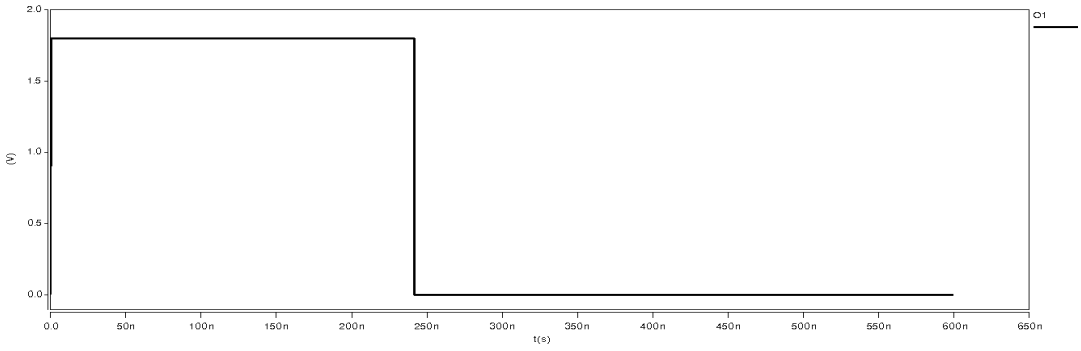


(g)

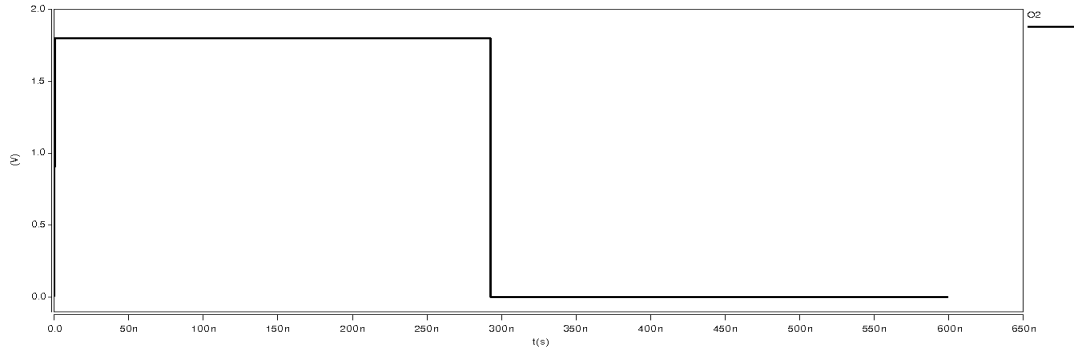


(h)

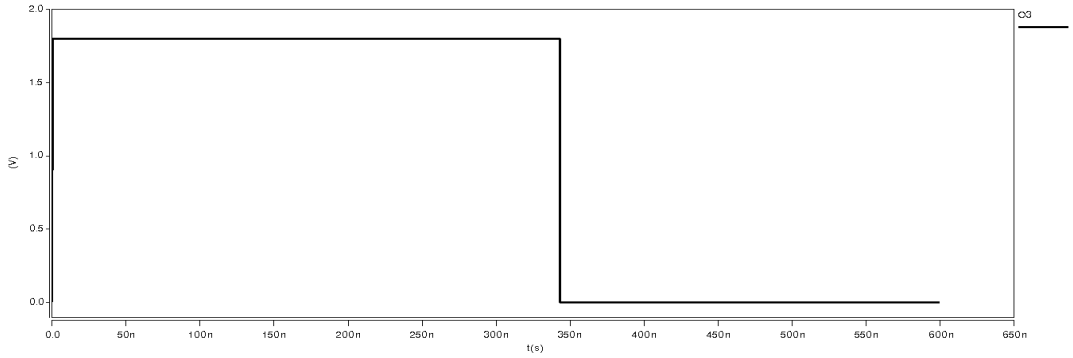
Figure 7. The capacitors across voltages waveforms (a) C_k, (b) C_1, (c) C_2 (d) C_3, (e) C_4, (f) C_5, (g) C_6 and (h) C_7


O1
2.0
1.5
1.0
0.5
0.0
(V)
0.0
50n
100n
150n
200n
250n
300n
350n
400n
450n
500n
550n
600n
650n
t(s)

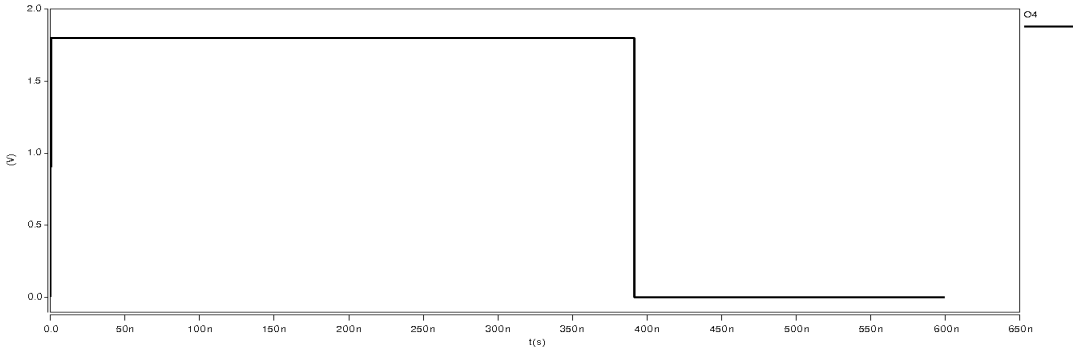
(a)


O2
2.0
1.5
1.0
0.5
0.0
(V)
0.0
50n
100n
150n
200n
250n
300n
350n
400n
450n
500n
550n
600n
650n
t(s)

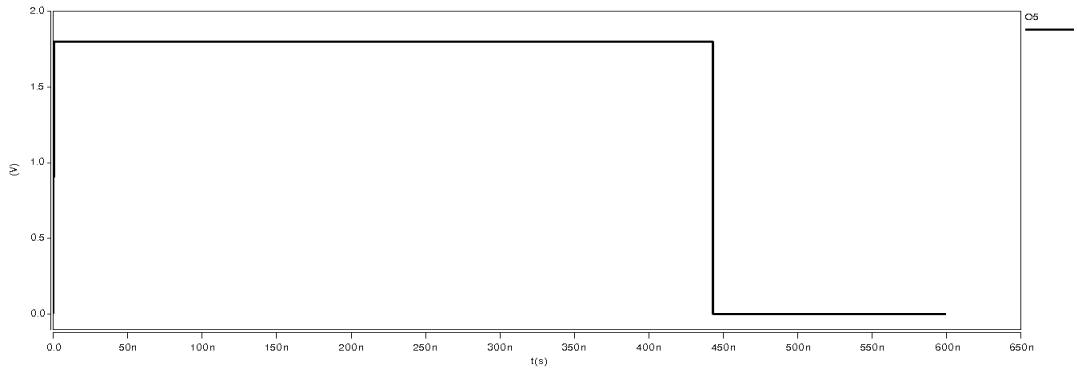
(b)


O3
2.0
1.5
1.0
0.5
0.0
(V)
0.0
50n
100n
150n
200n
250n
300n
350n
400n
450n
500n
550n
600n
650n
t(s)

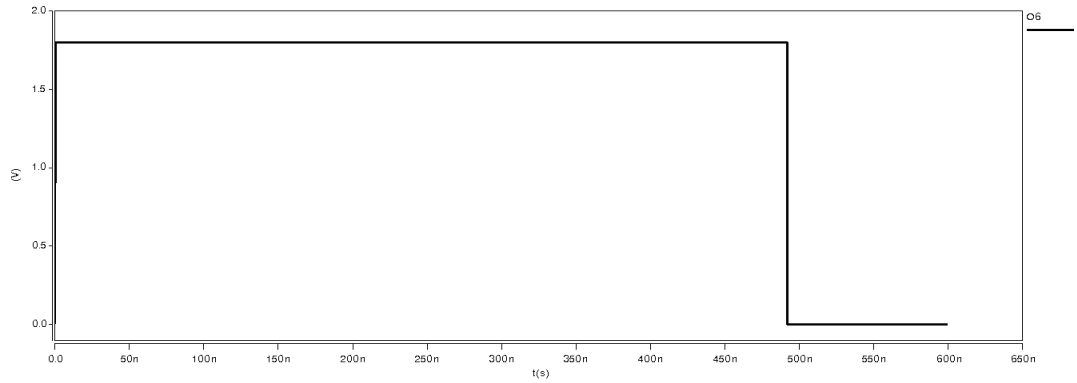
(c)


O4
2.0
1.5
1.0
0.5
0.0
(V)
0.0
50n
100n
150n
200n
250n
300n
350n
400n
450n
500n
550n
600n
650n
t(s)

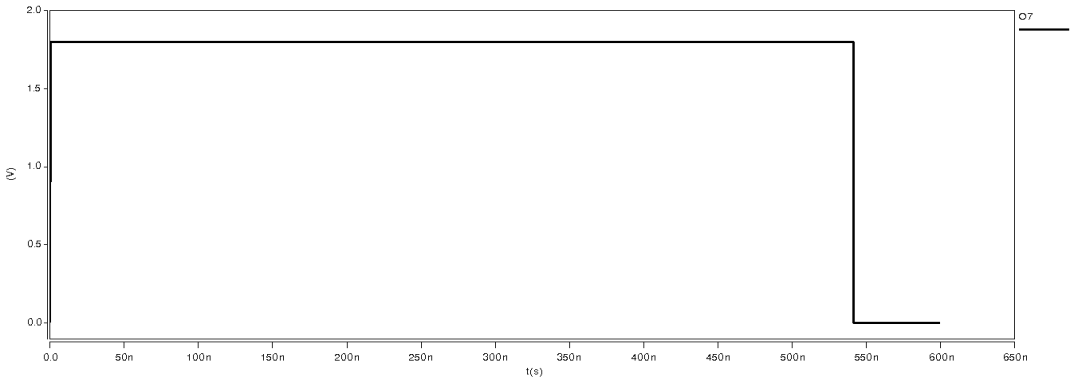
(d)



(e)



(f)



(g)

Figure 8. The comparators output waveforms (a) O_1, (b) O_2, (c) O_3, (d) O_4, (e) O_5, (f) O_6 and (g) O_7

low and D_{out1} is produced. As a result, the LSB or resolution in the simulated proposed converter is 1ns. The time resolution of the proposed converter is 264.5ps with corresponding stretch factor 50. The stretch factor is higher; the time resolution of the proposed converter is improved.

CONCLUSION

A new flash TDC has been developed using time interpolation and time stretching techniques which digitizes the time interval input signals and increases the resolution. This converter uses the dual slop conversion to increasing the resolution. The proposed converter eliminates the comparator offset voltage error and comparator parasitic capacitors error. Due to the use of flash structure, the proposed converter has advantage high conversion rate. Other proposed converter's features are low sensitive to the temperature; power supply and process variations (PVT) and eliminating the mismatching errors. Therefore, this converter is useful in high speed and resolution applications. The proposed TDC has been simulated by Hspice in TSMC 0.18µm CMOS technology. Comparison of the theoretical and simulation results confirms the proposed TDC operation.

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