



**FULL LENGTH ARTICLE**

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## **Design of an ECG Signals Amplifier with programmable Gain and Bandwidth Based on a New Method in Pseudo-Resistor Circuits**

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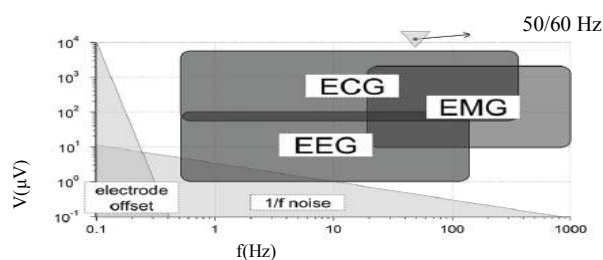
### **ABSTRACT**

*In this paper, an amplifier is designed in the 0.18  $\mu\text{m}$  CMOS technology for biomedical applications. The gain and bandwidth of the amplifier is digitally programmable. The amplifier consists of two stages. The low cutoff frequency is tuned in the first stage by a pseudo-resistor and it can be adjusted from 0.25 Hz to 9.8 Hz. The high cutoff frequency is also adjusted by proper selection of capacitors at the output of the first stage and it can be changed from 46 Hz to 334 Hz. The overall gain of the amplifier is programmed in the second stage. This is achieved by choosing the right values of capacitors in the input path of the second stage. The supply voltage in this circuit is 1 V and the integrated input referred noise is as low as 3.48  $\mu\text{V}_{\text{rms}}$  over the bandwidth the amplifier (from 0.25 Hz to 334 Hz) and the total power consumption has been measured to be 162 nW.*

**Keywords:** Programmable gain, programmable bandwidth, bio-potential signal amplifier, CMOS technology, sub-threshold, pseudo resistor.

### **INTRODUCTION**

In amplifiers with digitally programmable gain and bandwidth, gain and bandwidth are adjusted and optimized by signal receiver that is usually a processor. Types of digital processing on these signals such as digital filters, intelligent detection of unusual electrocardiography (ECG) signals, sampling ECG signals of patients during activity and carrying out daily activities and etc are various applications in which the sampling and the recording of ECG signals arise with the best quality. These amplifiers can have a significant impact on the quality of sampling the signals [1]. The difference in the bandwidth of bio-potential signals such as cardiac, nervous, muscular signals and etc, and also the difference in the amplitude of the received signals from the sensors can be the main reasons for using these types of amplifier in biomedical systems [1-2]. For example, the ECG signal amplitude may vary between 80  $\mu\text{V}$  and 2 mV [3]. Figure 1 shows the difference between cardiac signals and other bio-potential signals.



**Fig. 1. Frequency and amplitude characteristics of bio-potential signals [2]**

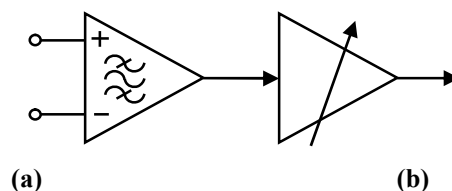
These types of amplifiers can be used to transmit a received ECG signal and in telecommunication and wireless applications, and to receive a high quality signal at the receiver too [4]. On the other hand, using these amplifiers can be beneficial in ECG signals measurement systems that use analog to digital converter (ADC) block, for applying an acceptable signal to ADC and digital and optimal gain adjusting [5-6]. More importantly, the different types of human skin (children, middle-aged and elderly) and the nature of the human body, the presence of noise on the skin surface, different types of connecting wires to transmit signals to amplifiers and natural error of connecting electrodes to the skin, especially in the electrodes with gels, can be good reasons for using these types of amplifiers to achieve the acceptable range for applying the receiving signal to ADC module.

One seemingly important issue in the biomedical integrated circuits manufacturing is the rejecting of low frequencies from the muscles movements that are received by sensors connected [7]. In order to eliminate these frequencies of the amplifiers, a low-pass filter with adjustable low cutoff frequency is usually used. This method eliminates the disadvantage of using large capacitors in integrated circuits due to enlargement of the chip [6-7]. In this paper, a new adjustable pseudo-resistor, with much smaller area and simpler structure is proposed that can digitally adjust the low cut-off frequency. High cut-off frequency can also be tuned by selective parallel capacitors structure, to properly receive the signal for the desired medical application.

Minimizing power consumption and integrated input referred noise, are other important issues in medical integrated circuits, because in integrated circuit amplifiers, power and input noise are in opposition. The optimal design will be achieved when input noise is minimized where power consumption is low [5-7]. In this paper, focusing on reducing the supply voltage and power consumption, and to reduce the battery size and lifetime in portable biomedical amplifiers, and reducing the input noise, the transistor inputs in the first and second stages, are biased in the sub-threshold region. This factor can be reduced the input noise effects and power consumption in the proposed amplifier.

The amplifier consists of two low-power and low-noise blocks. In the first stage, the bandwidth of the circuit is digitally adjusted by tuning the low and high cutoff frequencies. This structure can be used in selecting the signal desired type, and selects the medical application requirements. The second class, the overall gain is digitally adjusted for amplifying ECG signals with different amplitudes which have been received from various sectors.

The second stage is designed that there is no effect on the high cutoff frequency of the circuit. Since connecting the output to ADC circuits, with different input capacitors may change high cutoff frequency and bandwidth amplifier consequently. Thus, in the second stage, regardless of the size of the output capacitor, the gain is adjusted by the capacitors structure in the input path. Figure 2 shows the proposed architecture of the amplifier that the components are separately examined next.



**Fig. 2. Proposed architecture of Programmable Amplifier, a) First stage amplifier with tunable bandwidth, b) Second stage amplifier with tunable gain**

### Theorem

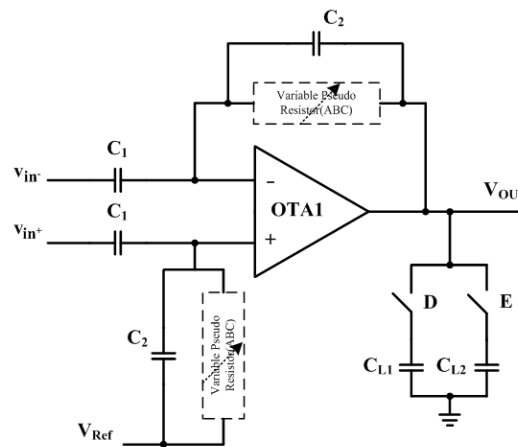
In the proposed designed amplifier, adjusting the gain and bandwidth are intended individually in two stages. Input signal from the input sensors is applied to the first stage, required harmonics of the input signal are amplified signal in this stage and the amplified signal is sent to the second stage. In second stage, the input signal is amplified as required and appears as the output.

### First stage amplifier

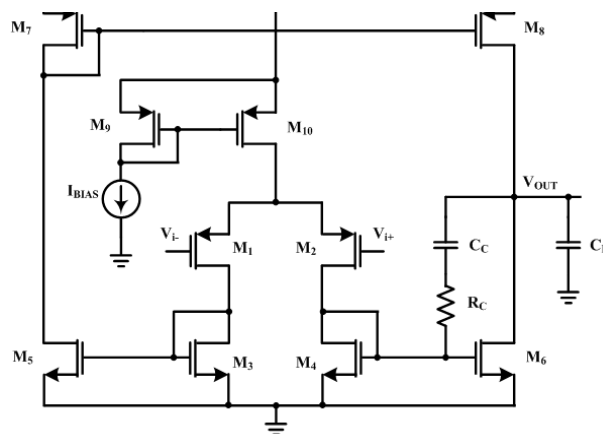
As shown in Figure 3, this stage is designed of current mirror amplifier and a high-pass filter (one in the feedback path and the other in the amplifier input). In this amplifier,  $V_{Ref}$  regulates DC output voltage. This voltage to achieve maximum amplitude at the output is set  $V_{DD}/2$ . The low cutoff frequency of the circuit is obtained from the following equation:

$$(1) \quad f_L = \frac{1}{2\pi R_{Pseudo} C_2}$$

Where  $R_{Pseudo}$  is the resistance value of the pseudo-resistor that can be set up to over  $1\ T\Omega$ , and  $C_2$  is the capacitor in parallel with pseudo-resistor. In previous figure, the proposed combination of the adjustable pseudo-resistor and the parallel capacitor ( $C_2$ ) composes the high-pass filter (HPF). Achieving to high resistance value and adjustable in this combination, has eliminated the use of large capacitors in the low-pass filter. The amplifier mid-band gain is easily obtained as  $A_m = C_1/C_2$ , where  $C_1$  is the input capacitor and  $C_2$  is the capacitor of the feedback path shown in Figure 3. High cut-off frequency of the circuit can also change by selecting output amplifier capacitors based on the application requirements. This frequency can be calculated and designed using the equation  $f_H = g_m/2\pi C_L A_m$ , where  $g_m$  is the transconductance of the input transistors and  $C_L$  is the OTA output capacitor. Increase in  $g_m$  resulted from the increased bias current of the amplifier can also increase the high cut-off frequency, but since this paper is to focus on reducing the power consumption, change the output capacitors method is used.



**Fig. 3. Schematic of the first stage amplifier with tunable bandwidth**



**Fig. 4. Current mirror amplifier circuit diagram [9]**

### Current mirror amplifier

One problem of the ECG signals amplifiers is the presence of noise at low frequencies and bandwidth, when achieving the minimal power consumption. Achieving low noise and low power consumption is always a big problem in the design of biomedical signal amplifiers [8]. To eliminate the problem, can choose the appropriate ratio of  $W/L$  in the input transistors of the differential stage and design the transistors in sub-threshold region. This type of arrangement can also reduce the noise input. On the other hand, designing transistors in the sub-threshold region, the minimum operating voltage can be achieved, resulting in lower power consumption. Figure 4 shows the designed current mirror amplifier.

In this circuit, transistors  $M_1$  and  $M_2$  work in the sub-threshold region, where  $g_m$  and  $I_D$  have linear relationship with each other, while in the saturation region,  $g_m$  is proportional to the  $I_D$  square root. This means that one can achieve the desired  $g_m$  by minimum current, and in this case the minimum bias current and thus the low power consumption will be achieved. The following equation shows the relationship where  $N$  is the sub-threshold factor usually considered between 1.3 and 1.5 and  $V_T$  is the thermal voltage [9].

$$(2) \quad g_m = \frac{1}{NV_T} I_D$$

Input thermal noise at current mirror amplifier can be calculated from the following equation. In which  $g_m$  is the transconductance,  $\Delta f$  is the bandwidth,  $K$  is the Boltzmann constant and  $T$  is the noise temperature. As can be inferred from equation (3), to minimize thermal noise,  $g_{m1}$  should select as large as possible and  $g_{m3}$  and  $g_{m7}$  as small as possible. But  $g_{m3}$  and  $g_{m7}$  should not be very small, since the other parameters in the amplifier including phase margin, system stability and even output voltage range may be affected.

$$(3) \quad V_n^2 = \frac{16KT}{3g_{m1}} \left(1 + \frac{2g_{m3}}{g_{m1}} + \frac{g_{m7}}{g_{m1}}\right) \Delta f$$

In this amplifier, unity gain bandwidth (UGBW) frequency is obtained from the equation  $g_{m1}/C_L$ , while there are also two non-dominant poles  $g_{m3}/C_3$  and  $g_{m7}/C_7$  where  $C_3$  and  $C_7$  are gate capacitors of transistors  $M_3$  and  $M_7$ , respectively. The size of the transistors must be carefully determined to the poles be larger enough than UGBW, so the coefficient of  $W \times L$  in the transistors  $M_3$  and  $M_7$  should be so small to produce a smaller equivalent capacitor. Increasing area of the input transistors can reduce flicker noise, in addition to work the transistors in the sub-threshold region [10].

### Adjusting the low cutoff frequency

As seen in Figure 3, the combination of an adjustable pseudo-resistor and a capacitor, can be used to reject low frequencies below 1 Hz. Frequency harmonics caused by the patient respiration and muscle movements and etc., which can be seen in the received ECG signal, can be rejected by the filter. Figure 5 shows an example of a pseudo-resistor with large, constant and balance resistance value. According to the figure, the maximum value of the resistor will be around 1 G $\Omega$  based on the designed dimensions.

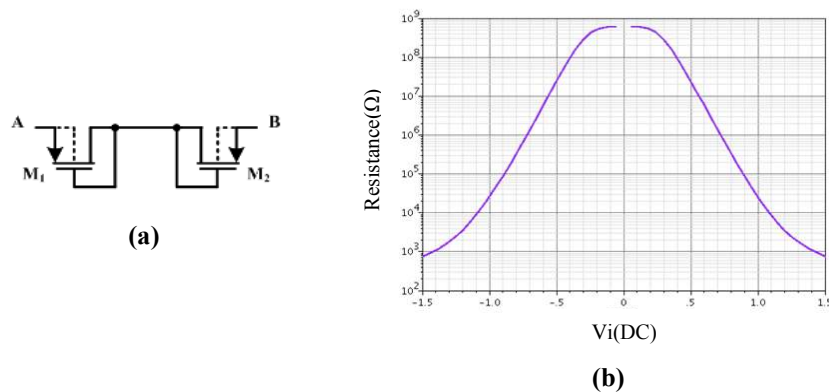


Fig. 5. a) Fixed balanced pseudo resistor, b) Simulated resistance of the (a)

In part (a) of the figure, if  $V_{SG} > 0$ , the transistor is at PMOS diode state and if the voltage is negative, the transistor exits PMOS state and the drain-well-source acts as PNP transistor, so the transistor acts as a BJT diode [11-12]. Accordingly, one can assume that if the transistor is mostly worked in the reverse diode region, the resistance value increases. In Figure 6, three new combinations of adjustable pseudo-resistors are provided. A floating voltage source  $V_B$  is used for their resistance values to be adjustable, that the  $V_B$  goes on to be replaced by a circuit.

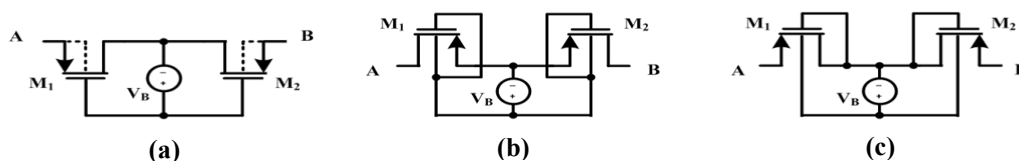
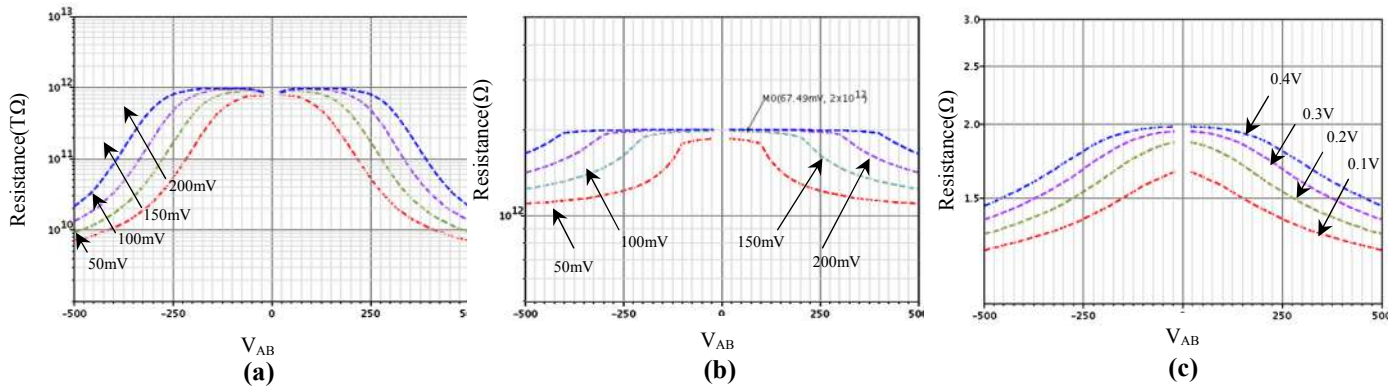


Fig. 6. Schematic of the proposed three pseudo resistors

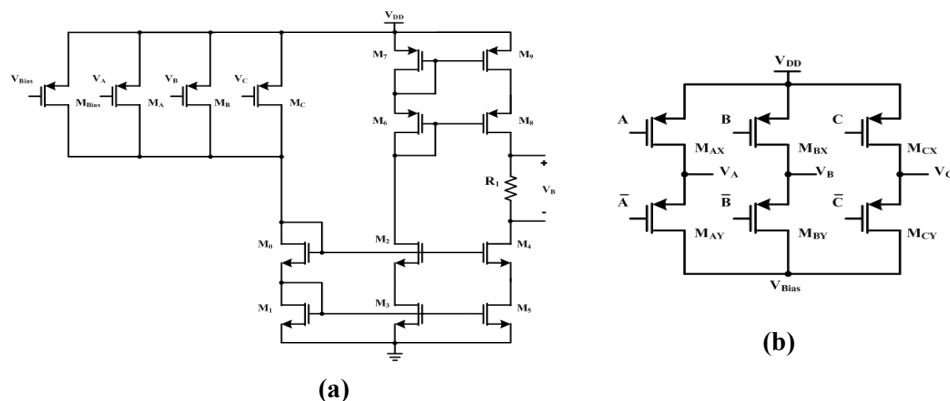
In Figure 6-(a), the potential supply voltage  $V_B$  can tune the resistance value of pseudo-resistor by more than  $1T\Omega$ . In Figure 6-(b), by changing the transistors as Dynamic Threshold metal oxide semiconductor (DTMOS), the linear range of the resistance value of the pseudo-resistor increases, but the resistance value does not change too much. In Figure 6-(c) where  $V_B$  source is applied directly to the bulk of the transistor, the change in value compared to the two previous cases, has increased. Simulation results of the three proposed combinations can be seen in Figure 7.



**Fig. 7. Simulation results of proposed three pseudo resistors, a) resistance curve of 6-(a), b) resistance curve of 6-(b), c) resistance curve of 6-(c)**

Among the three proposed simulations, Figure 6-(c), due to its large resistance value range and also linearity compared to other pseudo-resistors, can be better used to adjust the low cut-off frequency. As seen in the figure, the value can be increased by  $2 T\Omega$  in the Figure 6-(c). Figure 6-(b) can also be used in circuits where the input voltage is higher, and a constant and large resistance value is required.

$V_B$  floating voltage applied to the proposed pseudo-resistor shall be selected in practice by applying digital codes by the operator, and adjusting voltage by the above method is not reasonable. Hence, it is suggested, a circuit should replace the logic that can change its output voltage by applying digital codes. This logic leads the output to be dependent on the parameters of transistors employed and they do not change much in the process corners. Figure 8-(a) shows the circuit. In this circuit, transistors  $M_{Bias}$ ,  $M_A$ ,  $M_B$  and  $M_C$  are placed as current source transistors.  $M_{Bias}$  transistor produces initial current to generate output voltage  $V_B$  by applying  $V_{Bias}$ . But transistors  $M_A$ ,  $M_B$  and  $M_C$  are turned on by applying ABC digital codes and increase current to further produce  $V_B$ .



**Fig. 8. a) Circuit diagram of the  $V_B$  adjustable, b) circuit diagram of the voltage controller**

Circuit diagram that can provide voltage required for transistors  $M_A$ ,  $M_B$  and  $M_C$  by applying ABC digital codes can be seen in Figure 8-(b). In this circuit by applying single digit logic to inputs A, B and C, the upper transistors are turned off and the bottom transistors are turned on. Therefore the voltages  $V_A$ ,  $V_B$  and  $V_C$  also become equal to  $V_{Bias}$  value, as the result the generated voltage has increased in the current source as the reference voltage, thereby the output voltage  $V_B$  will also increase. By applying digital zero logic, this time upper transistors are turned on and the lower transistors are turned off, as the result, the output voltages  $V_A$ ,  $V_B$  and  $V_C$  will be equal to voltage  $V_{DD}$ . Therefore, transistors  $M_A$ ,  $M_B$  and  $M_C$  are turned off and they will have an effect on the current and as the result  $V_B$  will not be affected.  $V_{Bias}$  is 0.5 V in the circuit.

In Figure 8, by selecting keys A to C, different currents pass through resistor  $R_1$  and it provides the potential required for changing  $V_B$ . This voltage can change resistance value of pseudo-resistor and thus by changing and increasing value of the resistance, the low cutoff frequency of the amplifier will be digitally adjustable.

### Adjusting high cut-off frequency

Selective capacitors structure in Figure 3 that is designed at the end of the first stage amplifier can digitally adjust the high cutoff frequency of the amplifier. Based on how the received medical signal quality is considered the combination can be used to adjust the high cutoff frequency, depending on the application. In some applications, such as detecting heart rate, the high-frequency harmonics are not required and an high cutoff frequency of 40 Hz is sufficient, but in some applications, more specifically, the higher harmonics of the received signals are needed [10-14 and 15]. Capacitors that are used and able to be implemented in these types of amplifiers to reduce the chip area occupied can be a metal-insulator-metal (MIM) or metal oxide semiconductor capacitor (MOSCap). For example, in 0.18 $\mu\text{m}$  TSMC technology, a MIM or MOSCap capacitor with 4pF capacitance, occupies as much as 25  $\mu\text{m} \times 20 \mu\text{m}$  area. Thus, it is expected that the chip size of the ECG signals amplifiers with adjustable gain and bandwidth that are designed for low frequencies have larger dimensions than other amplifiers.

### Second stage amplifier

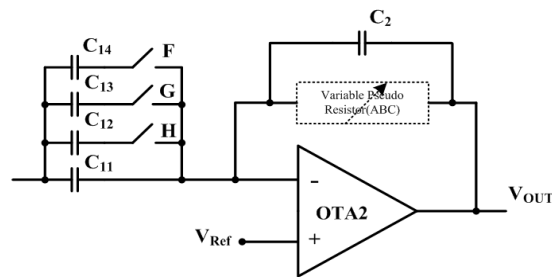
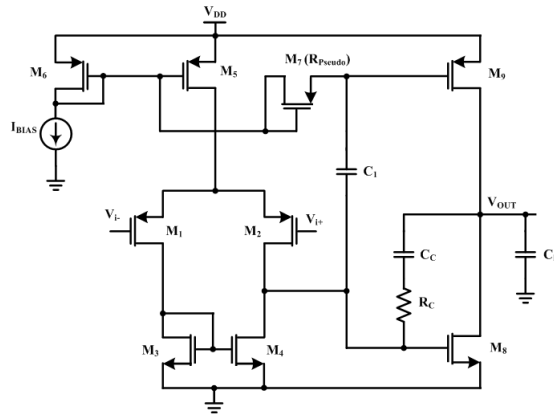


Fig. 9. Second stage amplifier schematic with gain adjustability

Schematic diagram of second stage amplifier can be seen in Figure 9. In this circuit, an AB class amplifier with a push-pull output consists the main part of the amplifier. The ratio of the total selective capacitors on the amplifier input to the feedback capacitor, specifies the gain value. High gain is not required in this stage, because the gain up to 65dB is sufficient in sensitive biomedical applications [14]. Pseudo-resistor-capacitor feedback is also designed to adjust the low cutoff frequency of the amplifier. It should be noted that the low cutoff frequency of the amplifier is adjusted simultaneously with the low cutoff frequency of the first stage, to create the greatest attenuation in rejecting lower frequencies. This factor leads to a drop in the frequencies by -40 dB per decade.  $V_{Ref}$  placed in the positive terminal of OTA<sub>2</sub> also regulates the output DC voltage. This amount is  $V_{DD}/2$  to achieve maximum and balance voltage swing at the output.

### Class-AB amplifier

Class-AB amplifier with push-pull output which can be seen in Figure 10, must have a high input signal range for receiving a signal from the previous stage. On the other hand, in order to further amplify the input signal, the amplifier must also have a high output voltage swing. If the amplifier output is connected to ADCs (due to the high input capacitance of the ADCs) slew rate of the amplifier should be enough to drive the large capacitor at the desired input frequencies. The input noise and power consumption of the amplifier should be also minimized using appropriate design. In Figure 10, on the input stage, a differential amplifier with active load is applied, and at the output stage push-pull is used. Capacitor  $C_1$  transmits the AC signal to the gate leg of output PMOS transistor, and also prevents the interference between output DC voltage level of the input stage and the transistor. DC voltage of the transistor is supplied by the PMOS transistor path which is diode-connected to the transistor gate providing bias current. The transistor size that can be seen as a pseudo-resistor is so high that does not allow the DC current. Thus, two output transistors are different in DC, but similar in applying AC signal. Dominant pole frequency of the amplifier is obtained as  $g_{m1}/C_C$ . In other words, the frequency is not dependent on  $C_L$ , but related to the  $C_C$ . thus, changing the output capacitor cannot provide a change in the high cutoff frequency and phase margin of the amplifier that is desirable.



**Fig. 10. Schematic of the class-AB amplifier with push-pull output**

To achieve low input noise and power consumption of the amplifier, similar to the first stage current mirror amplifier, input transistors of the differential stage of the amplifier are worked in the sub-threshold region. Thus, it can be achieved as the area of transistors M1 and M2 grow. The following equation shows the relationship between thermal noise with other parameters of the amplifier.

$$(4) \quad \overline{V_n^2} = \frac{16KT}{3g_{m1}} \left(1 + \frac{2g_{m3}}{g_{m1}}\right) + \frac{8KT}{3} \frac{1}{g_{m1} (r_{o1} \parallel r_{o4})(g_{m8} + g_{m9})}$$

Where,  $g_m$  is the input transistor transconductance,  $r_o$  is the transistor output impedance,  $K$  is the Boltzmann constant and  $T$  is the noise temperature. As can be seen, addition of  $g_{m9}$  in the denominator shows that the input noise of the AB class amplifier with push-pull output, compared to a typical two-stage amplifier, will be reduced. Input noise in a typical two-stage amplifier is obtained from equation 5.

$$(5) \quad \overline{V_n^2} = \frac{16KT}{3g_{m1}} \left(1 + \frac{2g_{m3}}{g_{m1}}\right) + \frac{8KT}{3} \frac{1}{g_{m1} g_{m8} (r_{o1} \parallel r_{o4})}$$

As  $g_{m1}$  increases the input noise is reduced, that it needs to increase the bias current, that according to the amplifier design a compromise must be made between power and input noise to achieve low power consumption.

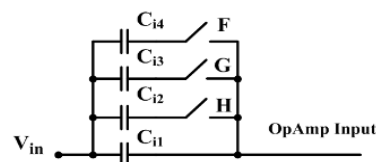
The voltage gain of the amplifier can be obtained from Equation 6. As it is known, the addition of  $g_{m9}$  to gain equation at push-pull output stage can increase the efficiency of the circuit, compared to the typical two-stage amplifier. In a typical two-stage amplifier, voltage gain is calculated from Equation 7.

$$(6) \quad A_V = g_{m1} (r_{o1} \parallel r_{o4})(g_{m8} + g_{m9})(r_{o8} \parallel r_{o9})$$

$$(7) \quad A_V = g_{m1} (r_{o1} \parallel r_{o4})g_{m8}(r_{o8} \parallel r_{o9})$$

Thus, in addition to reducing noise at the input of the circuit, achieving higher gain compared to typical two-stage amplifier, with regard to reducing the power consumption of the amplifier is not unavailable.

### Adjusting gain



**Fig. 11. The selectable capacitors to adjust the gain**

By selecting the capacitors placed in the feedback path and amplifier input, one can adjust the amplifier middle band gain calculating as  $A_m = C_i/C_2$ . It should be noted that  $C_2$  in the feedback network cannot be

changed due to placing at the HPF to eliminate lower frequencies. Thus, the idea of changing and selecting the input capacitors using controllable transistor keys is a good suggestion. Figure 11 shows the details.

The characteristics of these amplifiers define a parameter called noise efficiency factor (NEF) that better shows the relationship between noise and power consumption and the compromise between two parameters. This relationship that can be seen in Equation 8, determines how much power is consumed to reduce noise [14].

$$(8) \quad NEF = V_{n-in(rms)} \cdot \sqrt{\frac{2I_{tot}}{\pi V_t 4KT \cdot BW}}$$

where,  $V_{n-in(rms)}$  is the effective input noise voltage measured,  $BW$  is the amplifier bandwidth and  $I_{tot}$  is the current drawn from the power supply,  $T$  is the temperature in Kelvin,  $K$  is the Boltzmann constant, and  $V_t$  is the thermal voltage. Calculating the factor allows for the comparison between the power consumption and input noise of other similar circuits and the impact of design techniques used in the improvement of the parameters can be studied. The results of this study are presented below.

### Simulation results

In this paper after circuit simulation, first circuit simulation results at the first stage in order to achieve the adjustable bandwidth, and then the simulation results of the second stage to achieve an adjustable gain, and finally, the total simulation results of the amplifier were studied.

#### First-class circuits simulation

The current mirror amplifier in Figure 4 is first designed to achieve low power consumption. In the circuit, supply voltage is 1V, thus the current through the power supply is obtained 40 nA. Figure 12 shows the diagram of gain and phase of the amplifier. As seen in the figure, the gain is about 61.5 dB and the phase margin is measured 46°. In this case, power consumption is obtained about 40 nW. Integrated input referred noise is measured as low as 1.84  $\mu$ Vrms due to sub-threshold input transistors.

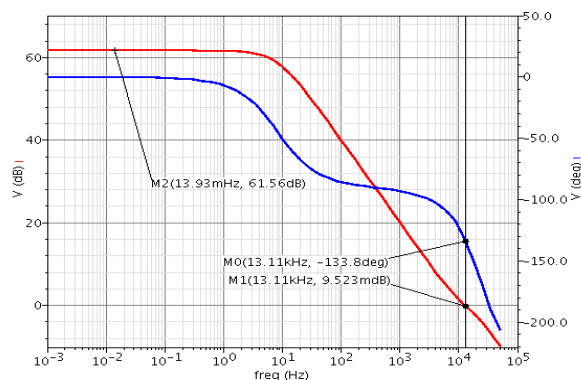


Fig. 12. Current mirror amplifier gain and phase curves of the first stage

#### Results of adjusting the frequency response at the first stage

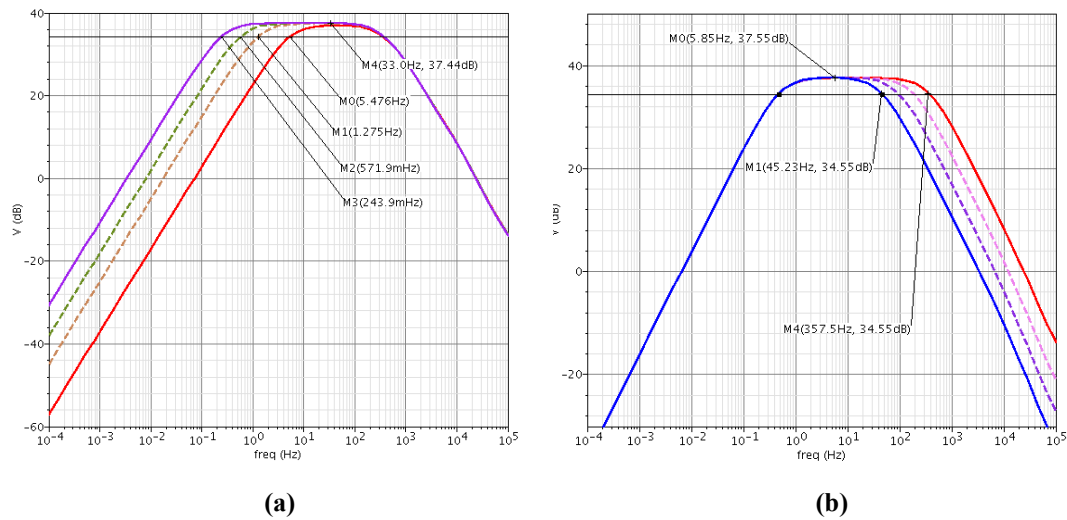
Table 1. Low cut-off frequencies for tuning  $V_B$  in fig. 8

Code (ABC)	$I_0$ (nA)	$f_L$ (Hz)
000	0.5	0.24
001	1	0.57
011	1.5	1.27
111	2	5.47

According to the description given in Figure 8, and the variable voltage  $V_B$ , the variable voltage is used to change resistance value of the pseudo-resistor proposed in Figure 6-(c). As a result, the low cutoff frequency at the first stage is digitally adjustable by changing ABC codes. Table 1 shows the details. Figure 13-(a), shows the frequency response of the first stage with adjustable low cutoff frequency with ABC codes. By selecting the first stage output capacitors in Figure 3, the high cutoff frequency of the first stage



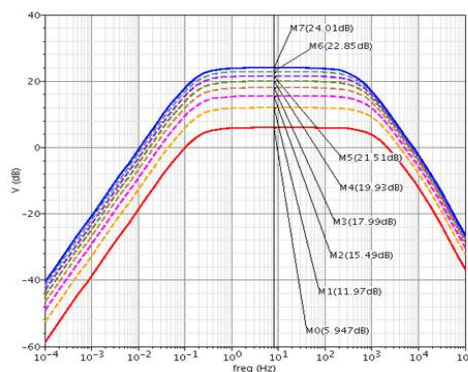
can also be adjusted. Figure 13-(b) shows the curve adjusting the low and high cutoff frequencies at the first stage.



**Fig. 13. First stage frequency response, a) low cutoff frequency adjusting, b) high cutoff frequency adjusting**

### Second stage circuits simulation

The second stage consists of three parts including class-AB amplifier with push-pull output, HPF and programmable gain part. HPF at this stage is adjusted along with the HPF at the first stage to apply attenuation of 40 dB/dec on the low frequencies of the input signals. At the simulation of class-AB amplifier with push-pull output, gain and phase margin are obtained 62.5 dB and 54°, respectively. In this case, power consumption and integrated input referred noise are measured about 114.6 nW and 1.26 μVrms. At the programmable gain part, the gain can be adjusted and optimized by selective capacitors. The desired gain can be adjusted by applying digital bits in three bits of FGH in Figure 9. In this figure, the values of capacitors C<sub>12</sub> to C<sub>14</sub> were 1pF, 2pF and 4pF, respectively. Capacitor C<sub>11</sub> is also considered 1pF. The second stage voltage gain can be adjusted to 8 different states, ranging from 6 dB to 24 dB. Figure 14 shows the adjusting.



**Fig. 14. Second stage gain adjusting curve using selecting input capacitors**

### Total simulation of the amplifier

In connecting stages to each other, the paper aims including adjusting the total gain of the circuit, adjusting the low and high cutoff frequency were simulated. The voltage gain is adjusted between 45.5 dB to 63.5 dB. The low cutoff frequency can be adjusted between 0.25 Hz and 9.8 Hz. The high cutoff frequency of output can be adjusted between 45 Hz to 334 Hz. Figure 15 represents the explanations. In Table 2, the results of the amplifier are reviewed along with the other results of the paper.

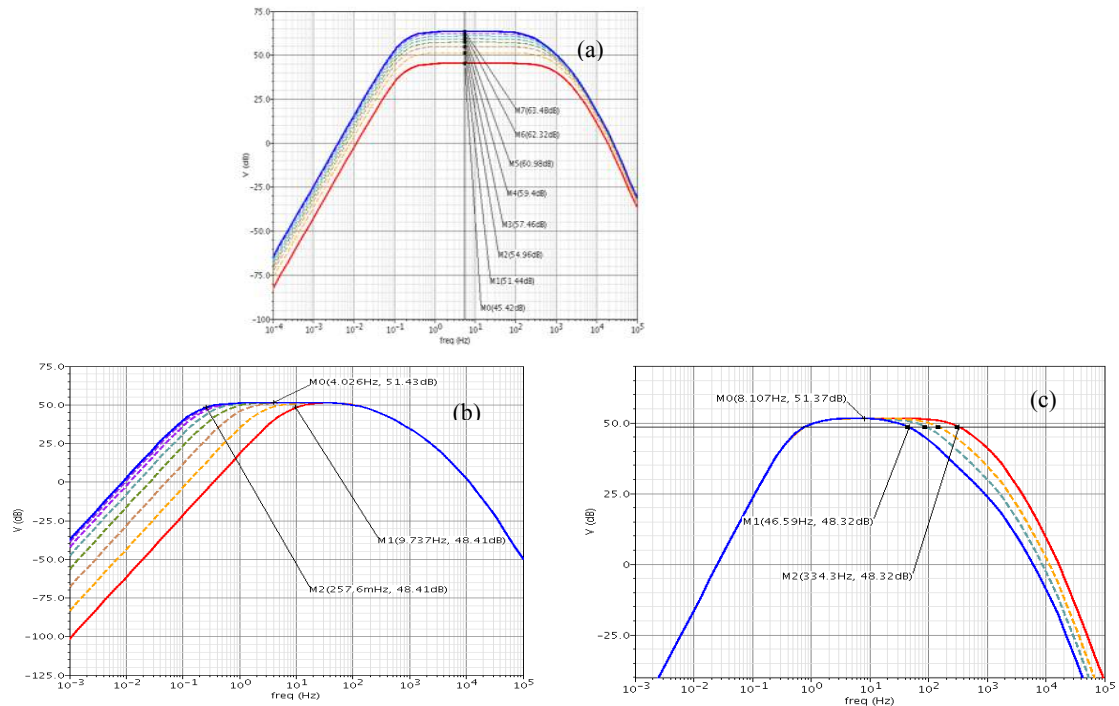


Fig. 15. a) overall gain adjustable simulation, b) low cutoff frequency adjustable in the output, c) high cutoff frequency adjustable in the output

Table 2. Comparison of several programmable gain and bandwidth amplifier performances

Parameter	[2]	[6]	[10]	[16]	[17]	This Work
Technology ( $\mu\text{m}$ )	0.5	0.18	0.35	0.18	0.13	0.18
Supply Voltage (V)	3	1	1	1.8	1	1
Bias Current (nA)	--	--	37-337	--	--	162
Gain Range adjustable (dB)	51.8-58-63.8-68	31-52	45.6-49-53.5-60	52.5-57.5	4 - 54	45.5-63.5
$f_L$ (Hz)	0.3-15.8	Adjustable	0.045-3.6	4-300	Adjustable	adjustable 0.25-9.8
$f_H$ (Hz)	40-350	Adjustable	31-92	Adjustable	Adjustable	adjustable 46-334
CMRR (dB)	110	100	71.2	88	--	88.5
PSRR (dB)	80	--	84	85	--	86
THD (dB)	-47	--	-44.4	-46	-43	-44.5
Output Voltage Range(V)	1.05-1.7	--	--	1	--	0.85
Input Referred Noise	$0.6\mu\text{V}_{\text{rms}}$	$1.9\mu\text{V}_{\text{rms}}$	$2.5\mu\text{V}_{\text{rms}}$	$2.6\mu\text{V}_{\text{rms}}$	$14.4\mu\text{V}_{\text{rms}}$	$3.48\mu\text{V}_{\text{rms}}$
NEF	--	--	3.26	3.38	--	2.92
Power	$60\mu\text{W}$	$36\mu\text{W}$	445nW-895 nW	$20.8\mu\text{W}$	$55\mu\text{W}$	$162\text{nW}$

## DISCUSSION AND CONCLUSION

In this paper, an ECG signals amplifier at low frequencies with programmable gain and bandwidth is designed and simulated. Three examples of new pseudo-resistors were proposed in this paper, of which one was placed in the circuit with a parallel capacitor as HPF due to its simple structure and adjustability, and a higher range of resistance value compared to other pseudo-resistor circuits. The pseudo-resistor with a value more than 2 T $\Omega$  could adjust the low cutoff frequency between 0.25 Hz and 9.8 Hz. The high cutoff frequency of the circuit could be adjusted between 46 Hz and 334 Hz by selecting output capacitors of the first stage. Overall gain was also available between 45.5 dB and 63.5 dB by using to selective capacitors at the input of the second stage. The total power consumption of the circuit by taking the output capacitor as  $C_L=10$  pF, was obtained 162 nW and integrated input referred noise of the circuit was obtained  $3.48 \mu\text{V}_{\text{rms}}$ . Calculating the NEF showed that the factor is lower than that of other similar work.

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